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Green Networking: Analyses of Power Consumption of Real and Complex IFFT/FFT used in Next-Generation Networks and Optical Orthogonal Frequency Division Multiplexing

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**UNIVERSITY OF
PLYMOUTH**
Doctoral College

***Green Networking: Analyses of Power
Consumption of Real and Complex
IFFT/FFT used in Next-Generation
Networks and Optical Orthogonal
Frequency Division Multiplexing***

by

Sameer Sami Hassan Al-Obaidi

A thesis submitted to the University of Plymouth
in partial fulfilment for the degree of

DOCTOR OF PHILOSOPHY

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Copyright Statement

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Authors Declarations

At no time during the registration for the degree of Doctor of Philosophy has the author been registered for any other university award without the prior agreement of the Doctoral College Quality Sub-Committee.

Work submitted for this research degree at the Plymouth University has not formed part of any other degree either at Plymouth University or another establishment.

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A programme of advanced study was undertaken, which included the extensive reading of literature, relevant to the research project and attendance at international conferences on Power consumption and communications.

The author has presented papers at the following international conferences:

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Abstract

The Orthogonal Frequency Division Multiplexing is a promising technology for the Next Generation Networks. This technique was selected because of the flexibility for the various parameters, high spectral efficiency, and immunity to ISI. The OFDM technique suffers from significant digital signal processing, especially inside the Inverse/ Fast Fourier Transform IFFT/FFT. This part is used to perform the orthogonality/De-orthogonality between the subcarriers which the important part of the OFDM system. Therefore, it is important to understand the parameter effects on the increase or to decrease the FPGA power consumption for the IFFT/FFT.

This thesis is focusing on the FPGA power consumption of the IFFT/FFT uses in the OFDM system. This research finds a various parameters effect on FPGA power of the IFFT/FFT. In addition, investigate the computer software used to measure and analyse the FPGA power consumption of OFDM transceivers, and selects the target hardware used in the computer software.

The researched parameters include the number of bits used in calculating the phase factor precision; Cyclic Prefix length effected on IP core IFFT, Subcarrier modulation type, word length width, Real and Complex Value IFFT, IFFT length, and subcarriers sampling frequency. The real value IFFT is proposed in 1987 and implemented in this thesis. These parameters above are discussed by comparing the result between the Real and Complex value IFFT used inside the OFDM system.

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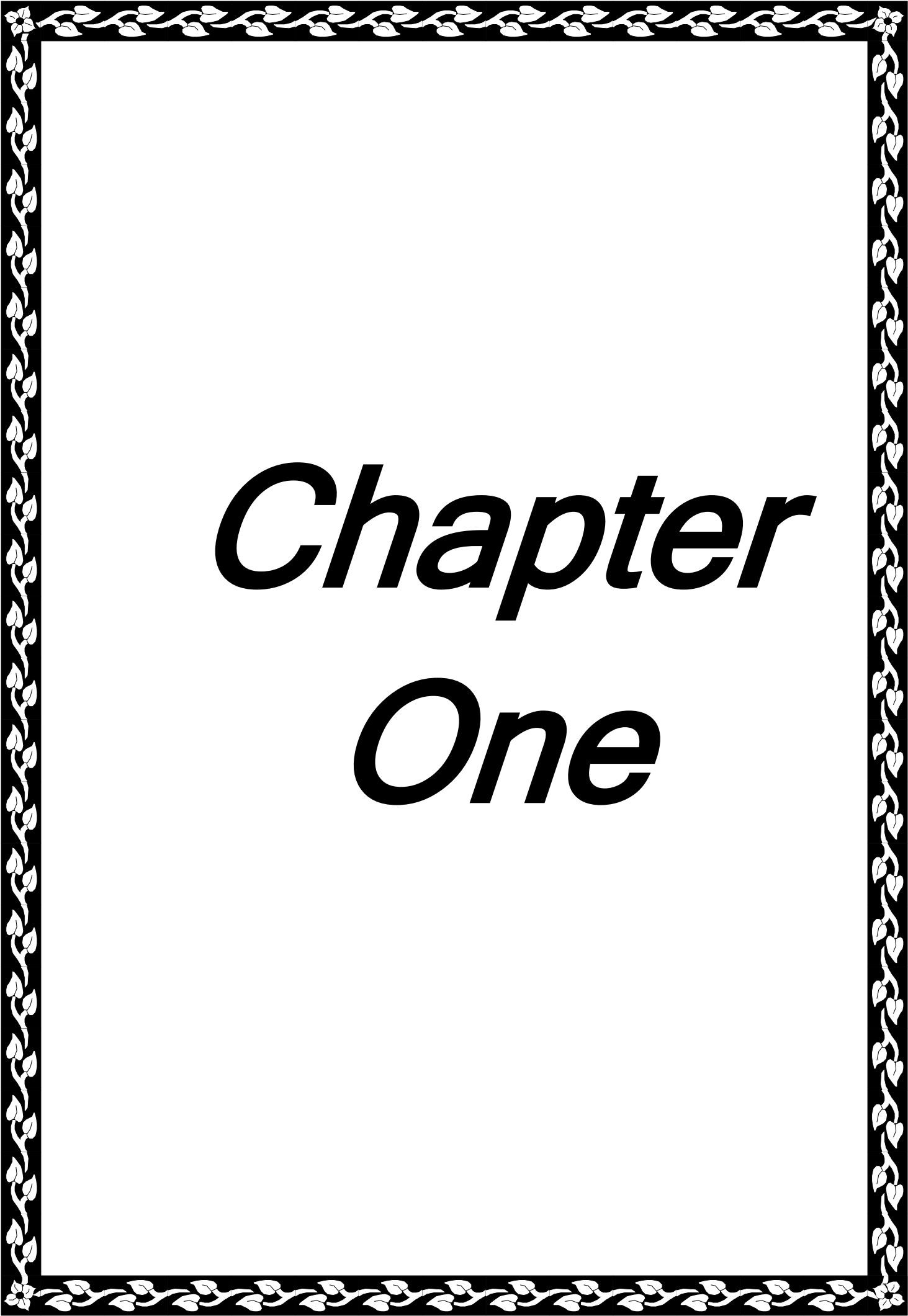
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Abbreviations

HCED	Higher Education for Education Development in Iraq
FPGA	Field Programable Gate Array
OFDM	Orthogonal Frequency Division Multiplexing
DSP	Digital Signal Processing
CP	Cyclic Prefix
ADC	Analogue to Digital Convertor
DAC	Digital to analogue Convertor
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
FMC	FPGA Mezzanine Card
XPA	Xilinx Power Analyser
ISI	Inter Symbol Interference
ISE	Integrated Synthesis Environment
XPE	Xilinx Power Estimation
IFFT	Inverse Fast Fourier Transform
FFT	Fast Fourier Transform
FCT	Fast Cosine Transform
IFCT	Inverse Fast Cosine Transform
NGN	Next Generations Network

DCT	Discrete Cosine Transform
IDCT	Inverse Discrete Cosine Transform
IDFT	Inverse Discrete Fourier Transform
DFT	Discrete Fourier Transform
NGOA	Next Generation Optical Access
DSNR	Dynamic Signal to Noise Ratio
SNR	Signal to Noise Ratio
BER	Bit Error Rate
ACP	Adaptive Cyclic Prefix
BL	Bit Loading
PL	Power Loading
BPL	Bit Power Loading
HSIC	High-speed Integrated Circuit
VHDL	Very HSIC Hardware Description Language
HDL	Hardware Description Language.
RTL	Register Transfer Level.
DDPD	Direct Detection Photo Diode
ICI	Inter-Carrier Interference
PON	Passive Optical Network
SMF	Single Mode Fiber

RDFT	Recursive DFT
rHDFT	Recursive hopping DFT
SDFT	Slide DFT
CRT	Chines Remainder Theorem
PFA	Prime Factor Algorithm

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Chapter

One

CHAPTER 1

INTRODUCTION

The modern way of living has created a significant demand for resources that are damaging the Eco-balance of the planet. The demand for the network bandwidth-hungry applications such as data centre is increased today [1]. This application is programmed in Integrated Circuit which operates inside electronic devices and consumes electrical power to satisfy the increasing demand described above[2].

The manufacturing of the electronic integrated circuit uses FPGA and programmed by Hardware Description Language. It has been predicted that the energy consumption of hg future networks will be a significant increase in the next few decades [3]. The challenge of the next-generation network is the power consumption for electronic circuits which required to build the network devices. Therefore, a simple solution towards a greener world would be by reducing the power consumption of electronic devices. Today the researchers are addressing this problem and target the power consumption for FPGA design circuits as a step towards greener network communication applications [4].

The OFDM is one of the most promising modulation techniques for next-generation networks due to high spectral efficiency, flexibility and immunity to ISI [5]. However, the OFDM techniques suffered from significant high complex Digital Signal Processing (DSP) operations which consume a significant amount of electrical power.

In the last decade, this technique has used a scheme of Frequency Division Multiplexing (FDM) as an essential modulation [6]. The development of FDM by orthogonal the subcarriers to each other uses IFFT/FFT (Inverse/Fast Fourier Transforms) which is one of the critical operations in OFDM and consumes a significant amount of FPGA power [7]. Moreover, the advantage of OFDM over a single carrier is a large number of adjacent subcarriers used to carry data which is divided into several parallel streams of data or channels. The time spaces between the subchannel $1/T$ Hz and sometimes the adjacent subcarriers in the symbol is overlapped in a time domain after IFFT. The solution to the above problem uses CP to eliminate ISI between symbols [8].

The various methods dealing with the understanding the OFDM power have been developed as in [9][10][11][12] and [13]. All these methods are focused on signal power, complexity and processing. The Fast-OFDM method uses IDCT/DCT to generate real OFDM symbol by using a Cosine part of the transform and developing it by uses IFFT/FFT. The Dynamic Signal-to-Noise Ratio (DSNR) method which finds the relation between SNR and Power consumption of the OFDM model [9] by controls the number of bits used in calculation precision.

The Adaptive Cyclic Prefix (ACP) method is focused on managing the length of the Cyclic Prefix to eliminate the delay, which causes a significant increase in dissipated channel energy and distortion[11][14]. Adaptive Loading Algorithms (ALA) methods are focused on individual OFDM subcarriers by selecting the best modulation format (from Binary Phase-Shift-Keying up to K-Quadrature Amplitude Modulation (K-QAM) and by adjusting the optimum power per subcarrier [15]. The purpose of this research to investigate the effect of the parameters on the FPGA power consumption of IFFT/FFT uses in the OFDM system. The researched results discuss the various parameters effected on FPGA power consumption. In addition, select the best computer software used to investigate the FPGA power consumption of IFFT/FFT which is Xilinx system generator.

This software is used to generate a power report for each experiment implemented in a different setting. The research includes the two OFDM model built real and complex value which depends on output from IFFT. The result compares the various parameters setting of the two OFDM model and discusses the FPGA power by using graph. The additional benefits of this thesis are simulated to built the transceiver transmitter of the OFDM system on one FPGA board. The previous researched study uses two board for the transmitter and the other for the receiver.

The next chapter presents an overview of different types of power consumption techniques, dealing with their strengths and weaknesses.

1.1 Definitions.

1.1.1 Static power

The power consumed while there is no circuit activity which caused by the current leakage through the device or defined as a power with no switching activity of the transistor inside the chips. This power type causes a leakage current inside transistor with no switching activity and correlates to FPGA area [16].

1.1.2 Dynamic power

The amount of power consumed by the device when it is actively operating or the power consumed by sources during transistors switching activity. The switching activity is defined as the number of signal transitions in a clock period [17]. The dynamic power is proportional to the frequency at which the supplies are running as well as the number of source unit used. The equation (1.1) represents the dynamic power [18].

$$\text{Dynamic Power} = \alpha CV^2f \quad (1.1)$$

α : switching activity.

C: loaded capacitance charging and discharging.

V: Power supply voltage.

f: clock frequency.

The dynamic part has two components:

- **Short circuit power** is due to the DC path between the supply rails during output transitions.
- **Switching power** is dissipated when capacitive loads are charged and discharged during logic changes.

1.1.3 Junction temperature

Each device is working according to the specific grade temperature in the datasheet. The background colour of the cell is turned to orange when the values are outside the range and turned red when it is outside the maximum range which may damage the device[19][20]. Finally, turned blue when set by the user.

1.1.4 Bit-Rate

The number of bits transmitted per second in the communication system from a transmitter to a receiver which defines the speed of the system. The Bitrate is calculated as in the equation (1.2) below for QPSK or QAM[21]

$$\text{BitRate} = \text{SymbolRate} \times \text{number of bit per symbol} \quad (1.2)$$

For OFDM, the symbol rate is calculated by other equations described in the next chapter.

1.1.5 Symbol-Rate

The symbols per second transmitted in the communication system is calculated by multiplying the number of the symbols by the sampling rate of the signal as in equation(1.3)

$$\text{Symbol rate} = \text{sampling rate} \times \text{Number of symbols} \quad (1.3)$$

1.1.6 Subcarrier

A subcarrier is one telecommunication signal carrier that is carried on top of another carrier so that effectively two signals are carried at the same time. At the receiving end, the main carrier and subcarrier signals are demodulated separately.

1.1.7 Digital Communication System

It is involved with transmitting information in a digital form. The essential elements of this system are the Transmitter, Channel, and Receiver. The information is passed from the transmitter to the receiver via transmission media channel [22]. The system as shown in **Figure 1-0-1**.

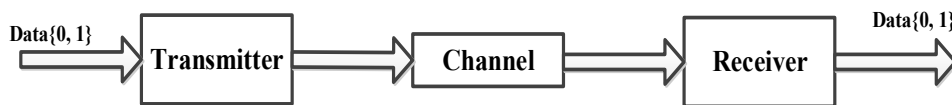


Figure 1-0-1 Digital Communication system.

1.1.8 Digital modulation

It is a generic name of the modulation, which is used to encode a carrier wave with the discrete signal. There are three types of digital modulation: Frequency Shift Keying (FSK), Phase Shift Keying (PSK), and Amplitude Shift Keying (ASK). Other types of modulation, combines the modulation types above to produce a QPSK and different order QAM. The basic idea behind the digital modulation is to get a high bit rate without increasing bandwidth.

1.1.8.1 QPSK modulation

The Quadrature Phase Shift Keying is a type of phase shift digital modulation. In QPSK the carrier is varied in phase, and there are four possible phase shifts. The separation in phase shift is $360^\circ/4=90^\circ$, so the four QPSK phase shift is $45^\circ, 135^\circ, 225^\circ$, and 315° each subcarrier represented by two bits that mean the representation as (00,01,10,11) [23].

The representation of the QPSK signal as shown in Figure 1-

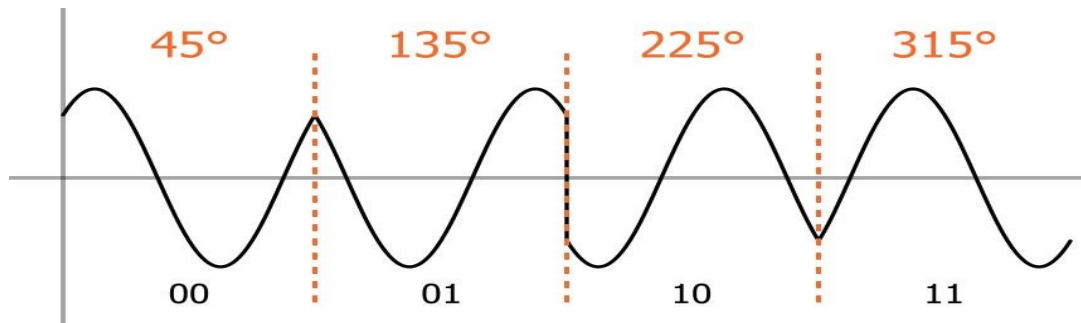


Figure 1-2 Format of QPSK signal

1.1.8.2 QAM modulation

Quadrature Amplitude Modulation is a type of digital modulation technique which combines both aspects of amplitude and phase modulation techniques for encoding signals [24]. The symbol state depends on the order of modulation for example 16-QAM it has 16 states, and each state is represented by 4 bits [24]. In general; the K in the K-QAM modulation represents the number of state of the symbol and $\log_2(K)$ represents the number of bit per each state in the Symbol. The advantage of the 16QAM over the QPSK is significant increase the amount of data rate by increasing the number of bits per Symbol [25].

1.1.9 Basic principle OFDM

The data rate is increased in the communication system to cover the applications used today [26]. The high data rate system suffers from a multipath fading channel, so the receiver is not able to track the different symbols due to the delays occurring in each separate symbol to copy the transmitted signal arrive at the receiver[27]. Therefore, a solution to the above problem by selecting the OFDM technique.

OFDM is a digital modulation technology used in many applications in wireless and wired communications. The OFDM symbol carries orthogonal subcarriers. OFDM is a particular case of FDM (Frequency Division Multiplexing).

1.1.9.1 History of development OFDM

The OFDM is the most popular transmission technique for a broadband communication system and had a long history of existence [28][29]. The first uses in transmission appeared in 1966 when Robert W. Change published his pioneering work on the synthesis of band-limited orthogonal signals for multi-channel data transmission [30]. The US military had uses OFDM in the high-frequency military system and variable data rate modem using DFT/IDFT [31]. The researcher introduced a CP extension in 1980 to reduce the ICI and ISI between subcarriers. The development continues using this technique in Optical Wireless Communication 2001 [32]. In 2005 the OFDM uses in optical fibre communication and 2009 in Coherent optical OFDM [33]. Additionally, in 2010 start targeting OFDM as a promising technology for the next generation Networks [29]. The development stage of OFDM techniques is shown in **Figure 1-3**.

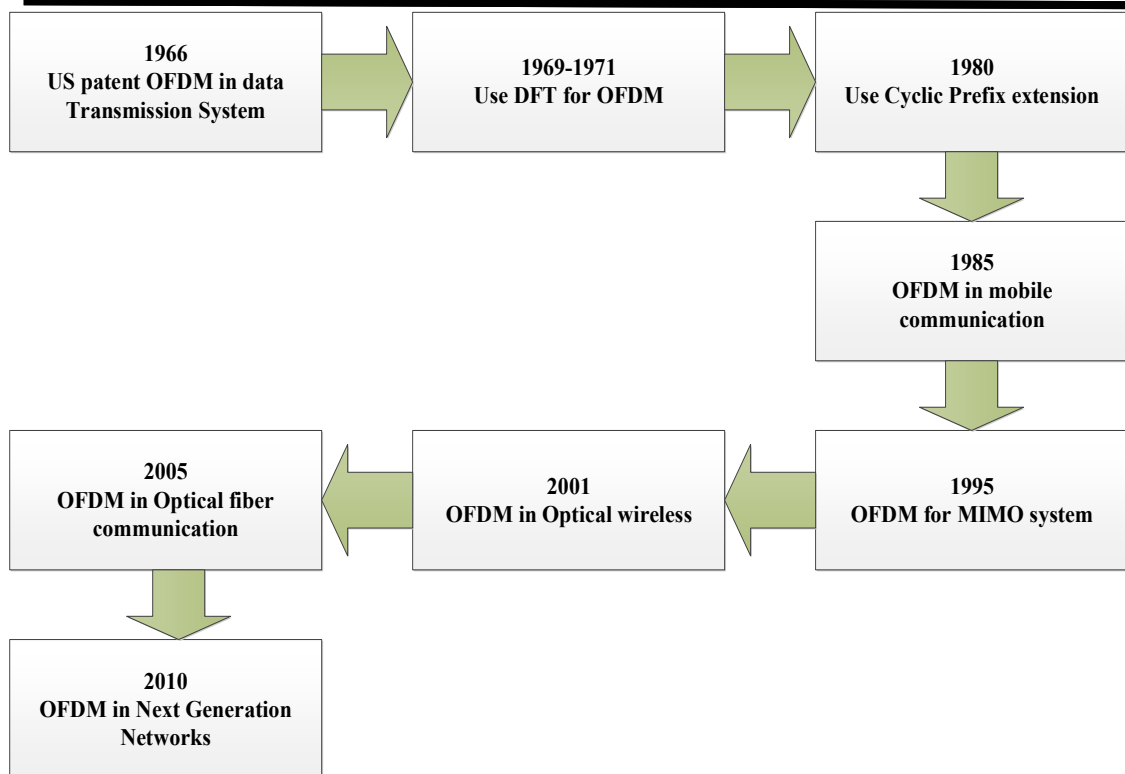


Figure 1-3 Historical OFDM development

1.1.10 FPGA (Field Programmable Gate Array)

The FPGA was invented less than 30 years ago, and it is fast growing in the different direction of engineering. The world first FPGA XC2064TM was introduced and shipped in 1985 by Xilinx. The FPGA was developed from 1985 to 2013 which grows 100,000 times in capacity and speed. There are two largest companies Altera and Xilinx which continue to dominate the market [34]. In general, the main components of the integrated circuit is the FPGA which programmed by the designer rather than the device manufacturer after manufacturing it and can Re-programme after deployed into a chipset IC [35]. The configuration of FPGA uses the Hardware Description Language (HDL) which is low-level description language for hardware.

The configuration resources to the FPGA provide a two-dimensional array implementing in a wide range of logic and arithmetic function. These resources include Multipliers, Dedicated DSP block, Dual port memories, Registers, Lookup tables (LUTs), Multiplexers, Tri-state buffers, Digital clock managers [36].

In addition, Xilinx FPGA contains an advance I/O mechanism that can handle a wide range of bandwidth and voltage requirement [37]. The configuration programme (HDL) download into FPGA through a static on-chip Random Access Memory (RAM) of the FPGA.

The Advantage of using FPGA is reduced non-recurring engineering cost which connected with a custom IC. It makes a shorter time to market and configuration ability of the FPGA and helps the designer to modify the design even after deployment in the end application [38].

The FPGA has freedom in implementing signal processing when using System Generator. The freedom means when defining data path widths throughout the system and employ much individual data processors by depending on system requirement [37]. The System Generator Provides an idea that allows a designer to design an FPGA by thinking about an algorithm that needs to implements [39]. However; an understanding of the FPGA algorithm, which gives the FPGA designer more capability to achieving high performance.

1.2 Thesis Aim and organisation

The aim of this thesis implements a proposed real value IFFT in OFDM model to generate a real value OFDM symbol. In addition, investigate and discover the effect of the various parameters on the FPGA power consumption of IFFT/FFT which is used in OFDM systems. The investigation depends on the previous research work that is discussed in the literature review. The researched parameters discover during the research such as the IFFT length, cyclic prefix length, real and complex IFFT, sampling frequency, modulation types, word length bits width, and bit precision. The procedure to estimate FPGA power consumption of the OFDM design model by using Xilinx system generator. The power report of the FPGA is generated for each Xilinx Simulink block with the various setting in the design and focusing on IFFT/FFT.

The OFDM design is implemented by Xilinx System Generator Simulink with Matlab code. The hardware target board is used a Xilinx Kintex-7 FPGA with High-Speed analogue daughter card (4DSP). The main idea behind using this type of hardware is to simulate the transmitter and receiver on one FPGA board instead of using two boards for the transmitter and receiver.

This thesis is organised into five chapters as it follows:

Chapter 2 Discusses the methods used to understand the power of the OFDM techniques which focus on two parts signal power and processing complexity.

The Fast-OFDM method focuses on generating the real output signal from IFFT which used inside OFDM model. The Dynamic Signal to Noise Ratio finds the effect of the SNR on the power consumption of the OFDM system. This method includes the IFFT bit precision effect on OFDM symbol with SNR and modulation types.

The Adaptive Cyclic Prefix had discussed the improvement of the spectral efficiency and reducing the transmission energy by reducing the delay caused by fixed type CP. Adaptive loading algorithm improves bit power by applying different algorithms such as bit loading, power loading and bit power loading algorithms. Finally, this chapter discusses the Hermitian symmetry used to generate the real value output from IFFT and discusses the complex value IFFT used in conventional OFDM.

Chapter 3 This chapter discusses the computer software platform and tools used to generate the power report for the OFDM design, for both models complex and real value. The discussion includes various computer software, and tools used to implement the OFDM. In addition, the type of software used in this thesis with advantage and disadvantage of selecting it. The procedure of generating the FPGA power report and the estimation power by using the Xilinx System Generator ISE14.7 and the feature of using Excel spreadsheet from Xilinx.

Chapter 4 This chapter discusses the implementation procedure of the OFDM, and the result of the researched parameters effects on FPGA power consumption of IFFT/FFT by applying the different setting. The explanation of

the proposed real value IFFT/FFT used in the design of the real OFDM is discussed in this chapter.

In addition, this chapter includes the experimental work, model design, FPGA power consumption, and result discussion. The result is compared between two model built real and complex value OFDM and discovering various parameter effect on FPGA power consumption of the IFFT/FFT.

These parameters can be classified to the following: the real and complex IFFT output, phase factor bit precision, cyclic prefix length, IFFT length, sampling frequency, and modulation types. The discussion result includes graphs and equations analyses of the FPGA power consumption of one part of the OFDM model which is IFFT/FFT.

Chapter 5 the work presented in this thesis is concluded, and some suggestions for future work in this area are given.

1.3 Contribution to Knowledge

The following list summarises the main contributions of the dissertation.

1. Proposed a new real value OFDM by using a real value IFFT input which is the novelty of this work. The proposed model is not similar to Hermitian symmetry used to generate the real value IFFT and widely used in real value OFDM. The proposed model generate the real part of the subcarrier by double up the real part input feed to the IFFT and complex conjugate the imaginary part, but the two inputs location are set to zero for the two locations $X(0)=0$ and the $X(N/2)=0$. The output result is real value OFDM symbol, and the imaginary part is significantly small and can be neglected.

2. Investigations, critical discussion and comparison of the various methods which deal with OFDM signal and processing power. It is the first researched study of the power method used in OFDM. This investigation is enabled to study the FPGA power consumption effect on IFFT/FFT with the effect of various parameters. Those methods can be categorized to the following: The method is focused on the complexity and signal type output from IFFT and input to FFT such as Fast-OFDM. This method is generated a real value output from IFFT instead of the complex value output from IFFT. The Dynamic Signal-to-Noise ratio (DSNR) is focused on the bit precision and modulation type effected on the power consumption of the OFDM model system. The researcher of DSNR used two FPGA evaluation board in the implementation and focused on total FPGA power of the transceiver.

The Adaptive Cyclic Prefix (ACP) is focused on the effect of the CP on the channel energy. The Adaptive Loading Algorithms (ALA) method is focused on the bit power and subcarriers modulation type. Those methods are enabled to study the researched parameters effect on the FPGA power consumption of IFFT/FFT which is the central processing of OFDM. In addition, the method uses to generate the real OFDM symbol from IFFT which is the first step of comparison the FPGA power consumption of IFFT/FFT.

This Contribution was presented by the author and publish in the following conference:

Sameer Al-Obaidi, M. Ambroze, B. Ghita, Elias Giakoumidis and Athanasios Tsokanos “A Review on Power Consumption Reduction Techniques on OFDM”, 11th International Network Conference, INC2016, Germany, Frankfurt, July 2016.

3. The novelty of study had discovered the researched parameters such as length of IFFT/FFT which is affected on FPGA power consumption of the OFDM. In addition, find the procedure to generate a power report of the OFDM design by system generator design. The first study of FPGA power consumption for OFDM design model which is focused on IFFT/FFT length. It discusses an implementation method, and computer software used to generate the FPGA power report of the OFDM model.

The computer software used to design an OFDM model by Xilinx System Generator to investigate the length of IFFT effects on FPGA power consumption. The power consumption result significantly increases with increasing length of IFFT. The increased IFFT length will increase the number of subcarriers input to this part which is increased the length of the OFDM symbol.

In addition, discover the effect of junction temperature with the length of IFFT which led to increasing the junction temperature. The power report is generated using power estimation from Xilinx and using an Excel spreadsheet to analyse power consumption of the IFFT/FFT uses in the OFDM. The hardware selection in the simulation computer software is a Kintex-7 high-speed analogue with daughter card for ADC/DAC.

This Contribution was presented by the author and publish in the following conference:

Sameer Al-Obaidi, M. Ambroze, N. Outram, B. Ghita “*The IFFT/FFT variant parameter effect on OFDM power consumption*” “Recent Trends in Engineering and Technology”(RTET-17), 6th Paris International Conference, France, Paris, April 2017.

4. The novelty of this paper had investigated the effect of bit precision and CP length on FPGA power consumption of the IFFT/FFT. The investigation of the two researched parameter effect on FPGA power consumption of IFFT. The two parameters are a number of bits used in the phase factor bit precision calculation of IFFT/FFT and the Cyclic Prefix length used with IFFT IP core.

The result discovered shows the power significantly increases with increasing the number of bits used in the calculation of Phase factor. In addition, the length increase of Cyclic Prefix led to reducing the FPGA power consumption of IP core IFFT v7.1 and junction temperature. The researched parameter is discovered that the junction temperature is increased with increased number of bit precision.

This contribution was presented by the author and published in the following conference:

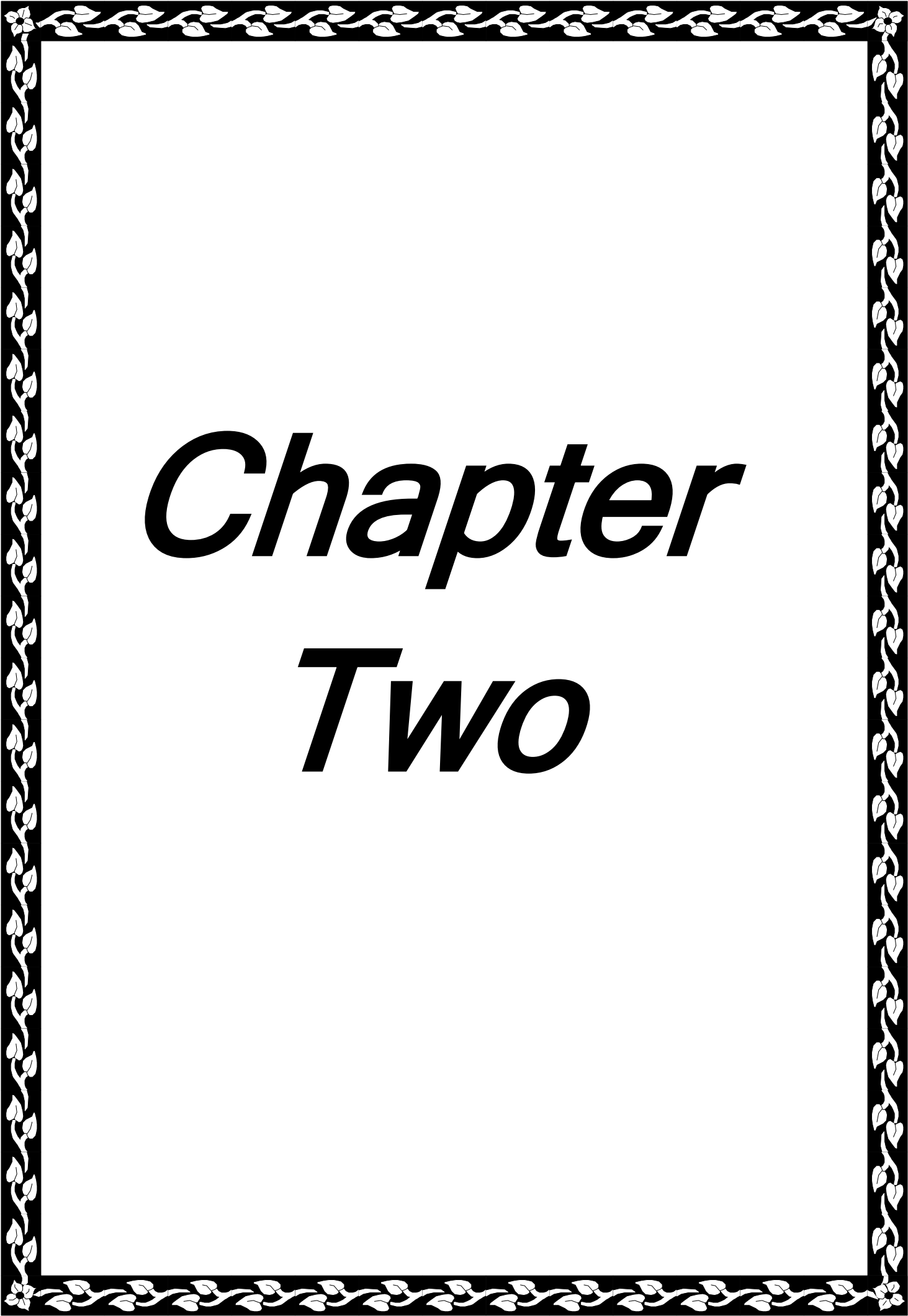
Sameer Al-Obaidi, M. Ambroze, N. Outram, B. Ghita “ Bit precision and Cyclic prefix effect on OFDM Power Consumption Estimation” ACM-2017 5th International Conference on Communications and Broadband Networking (ICCBN 2017), Bali, Indonesia.

5. The contribution of this research had discovered a parameter of OFDM symbol type or IFFT output type effect on the FPGA power consumption of IFFT. The result is compared between FPGA power consumption of real and complex value IFFT in OFDM model. The computer software uses a Xilinx System Generator Simulink to build the two OFDM models and generate the power report. The power report generated results finds the power consumed in a real value IFFT is lower than complex IFFT.
6. The contribution of this study has discovered the relation between subcarriers modulation types input to IFFT to generate the OFDM symbol with FPGA power consumption.

The subcarriers modulation type such as QPSK or high order 16QAM which effect on a number of bit per OFDM symbol. The result finds the type of subcarriers modulation how affected the FPGA power consumption of IFFT/FFT. The Xilinx power report result shows the power of IFFT using 16QAM subcarriers is the same power when using QPSK subcarriers modulation for the same settings of the two model built. The difference is the QPSK subcarriers carry 2 bits, and 16QAM carry 4 bits per subcarriers. Therefore, the increasing number of bits per subcarriers input to IFFT led to an increase in the processing of IFFT and the FPGA power consumption.

7. The contribution of this study has investigated the effect of subcarriers sampling frequency on FPGA power consumption of the IFFT used inside OFDM model. The sampling frequency increase of the input subcarriers led to reduce sampling time and increase the subcarriers bandwidth. The increasing sampling frequency is led to increases in the subcarrier bandwidth. The power consumption report shows the power is significant increase with increasing sampling frequency for two types of OFDM model real and complex value. The comparison includes two types of subcarriers modulation (QPSK and 16 QAM).
8. The contribution of this study has investigated the effect of the subcarriers representation in computer software and effect on FPGA power consumption of IFFT. The word length bit width is used to represent the subcarriers in computer software as a number of bits and depends on the hardware type used.

The number of bits represents by word length bit width for the subcarriers input to IFFT and find the effect on the FPGA power consumption. The increasing word length width is led to increases in the FPGA power consumption of IFFT/FFT of two types real and complex value OFDM. The result of increasing the FPGA power because increasing the number of bits represent the subcarrier by word length bit width which increases the processing inside the IFFT/FFT.

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Chapter

Two

CHAPTER 2

2 INTRODUCTION

The OFDM modulation technique a promising technology for next-generation optical communications networks which is used in most broadband wireless and wired communication systems [40]. OFDM had a long history of a research study in the last decade. This chapter will discuss the research methods dealing with OFDM power but focus on signal power and complexity. In addition, it is included a discussion of the method used to generate the real-value OFDM signal, such as Hermitian symmetry. The Fast-OFDM uses the real signal part output from the IFFT in the OFDM transmitter and the input to FFT in the receiver. The DSNR finds the relation between the bit precision and adaptive modulation with a total power of the OFDM design and SNR. The adaptive cyclic prefix is used to control the length of CP to reduce delay in the channel and improve the channel transmission energy of the OFDM system. The three methods above uses in this research thesis to analyse the FPGA power consumption on IFFT/FFT of the OFDM model. Finally, the discussion includes the Complex value IFFT with an equation which is used in this thesis.

2.1 Fast OFDM

The advantage of the OFDM such as higher spectral efficiency and high resistance to ISI. In conventional OFDM, the two parts of the signal, real and imaginary, are used to represent the OFDM symbol and carry data. However, the Fast-OFDM uses only one part of the signal, the real part, to represent OFDM symbol [41]. The optical Fast-OFDM (Optical F-OFDM) was proposed in 2010 [42] to reduce the subcarriers spacing when compared with conventional OFDM.

The OFDM mathematical representation is shown by equation (2.1)

$$S(t) = \sum_{k=0}^{N-1} a_k e^{j2\pi \frac{k}{T} t} \quad (2.1)$$

This equation shows the subcarriers frequency gap is $1/T$ for OFDM when using standard input and output two parts.

However, the frequency gap in Fast-OFDM= $1/2T$ which is the half subcarrier spacing in conventional OFDM[43]. The equation of OFDM with half subcarrier spacing is written as in equation (2.2).

$$S(t) = \sum_{k=0}^{N-1} a_k e^{j\pi \frac{k}{T} t} \quad (2.2)$$

$S(t)$: Fast-OFDM symbol

a_k : Subcarriers

$e^{j\pi \frac{k}{T} t}$: Twiddle factor

The advantage of this method is to reduce the complexity when compared with conventional OFDM [44][45][46].

There are many methods used to implement the Fast OFDM such as using (Inverse Discrete Cosine Transform) IDCT. This part is used to do the multiplexing and demultiplexing between subcarriers to generate the orthogonality between input subcarriers which is shown in **Figure 2-1**. This model is processing only the cosine part of the signal to get the real output OFDM symbol [47] [48].

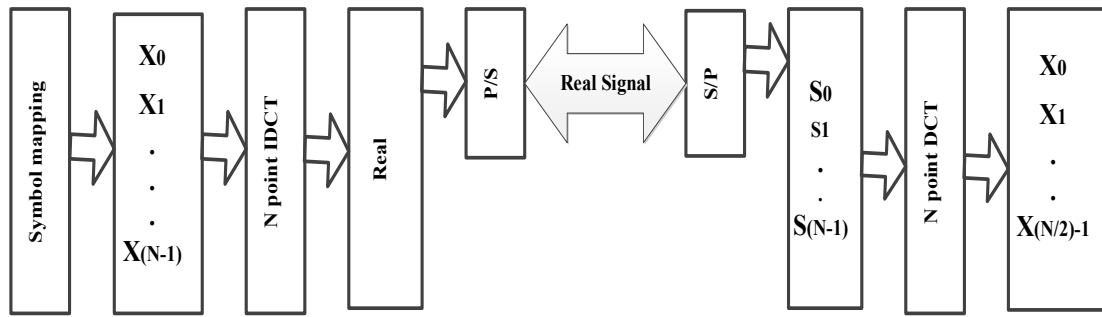


Figure 2-1 Fast OFDM by using IDCT/DCT

This transform type is slow when compared to fast algorithm IFFT/FFT. The IDCT/DCT is no more used in Optical Fast OFDM and replaced by more efficient and fast algorithm transform IFFT/FFT [49].

The one-dimensional equation of DCT is written as in the equation (2.3) [50];

$$X_c(k) = \frac{1}{N} \sum_{n=0}^{N-1} x_n \cos\left(\frac{2\pi kn}{N}\right) \quad (2.3)$$

$$K=0, 1, 2, \dots, N-1$$

The one dimensional IDCT equation is written as in equation (2.4)

$$x_c(k) = \sum_{n=0}^{N-1} c[u] X_n \cos(k2\pi n/N) \quad (2.4)$$

Where

$$K=0,1,2,3,\dots,N-1$$

X_n : DCT output.

$$c[u]=1 \text{ for } u=0$$

$$c[u]=2 \text{ for } u=1,2,3,\dots,N-1$$

The IDFT/DFT is used instead of IDCT/DCT then the size of the transform for multiplexing is increased to double ($2N$ IDFT) in the transmitter and ($2N$ DFT) in the receiver. **Figure 2-2** below shows the block diagram of using IDFT/DFT in the Fast-OFDM.

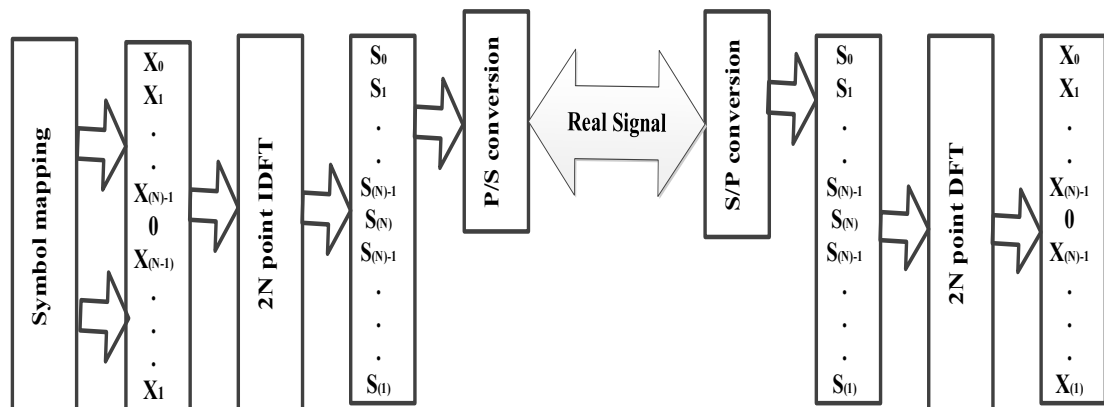


Figure 2-2 Fast-OFDM by using IDFT/DFT with Symmetric input

The IDFT/DFT is replaced by IFFT/FFT as a fast algorithm to implement the Fast-OFDM. The Fast-OFDM implemented by using Hermitian transform with IFFT to generate a real output signal. In addition, Fast-OFDM can be implemented by dividing the signal into real and imaginary, and each part divided into odd and even. The output symbol sequence is combined after a frequency shift to half the subcarriers spacing.

Then the imaginary part is up-converted to make sure there is no interference.

Each part (even and odd) of the subcarrier is used the IFFT to perform orthogonality between subcarrier [49][51] as shown in **Error! Reference source not found.**

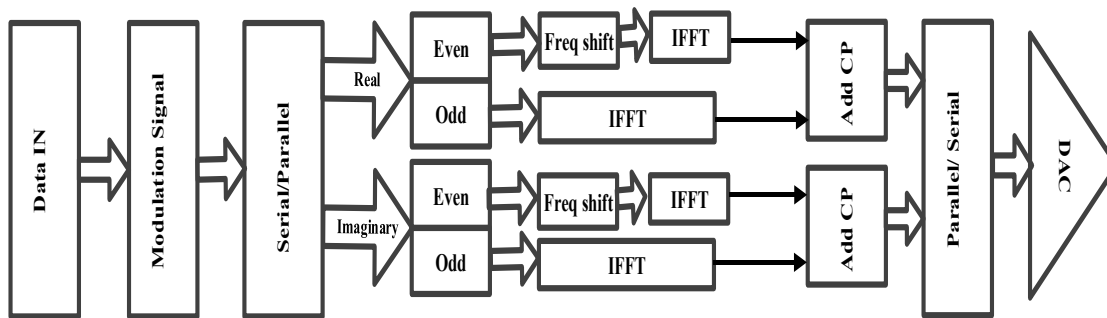


Figure 2-3 FAST- OFDM by IFFT/FFT

The Fast-OFDM method is used to generate a real OFDM symbol signal which used for optical transmission. This method has reduced the complexity and processing because generating one part of the OFDM symbol.

2.2 Dynamic Signal to Noise Ratio (DSNR)

The OFDM modulation techniques are selected as a promising technology for next-generation optical networks because of many advantageous features such as high network capacity, flexibility, high-speed, long reach, and energy efficiency [9]. The energy efficiency is an essential factor for the next-generation networks to get sustainable and green networks. However, the OFDM transceiver consumes significant energy due to having to perform complex Digital Signal Processing (DSP) operations.

The energy consumption because the complex electrical calculations operations inside IFFT/FFT to perform Orthogonality/De-Orthogonality between subcarriers to generate OFDM symbol. Therefore, DSNR method is an energy saving method used in real time FPGAs for Next generation optical networks. This method focuses on managing the number of bits uses in calculation precisions of IFFT/FFT function to satisfy optimum SNR (Signal to Noise Ratio) required for optimum bit error rate (BER) [10]. In addition, DSNR is related to the modulation format to satisfy BER (Bit Error Rate) requirement by control the number of bit in OFDM frame generation for adaptive modulation. The block diagram of Dynamic SNR is described in **Figure 2-4**.

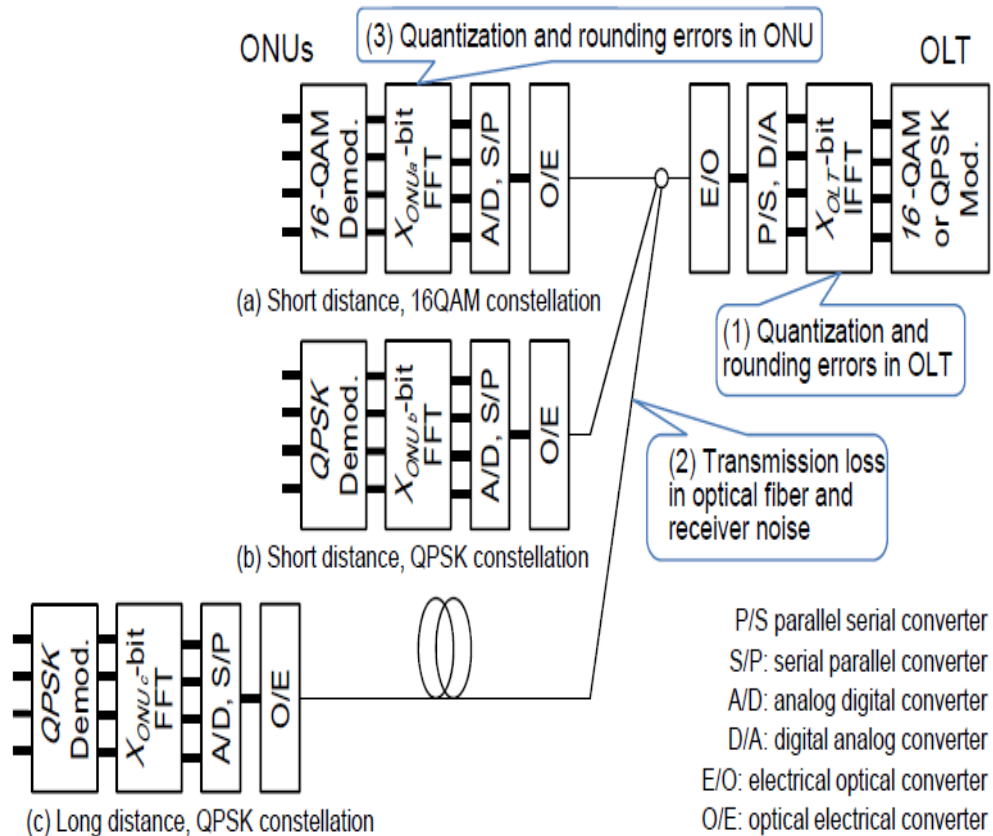


Figure 2-4 Dynamic SNR for OFDM-PON [52]

The dynamic SNR management defines the calculation precision according to the transmission distance when using the same constellation modulation.

If the transmission distance is short, the permissible FFT and IFFT calculation errors become large. In addition, upgrading the constellation modulation from QPSK to 16QAM improves the energy efficiency for a short-distance ONU, as shown in (a) in the figure above.

The experimental implementation [52] are used two Xilinx FPGA board type is Virtex-7 with A/D and a D/A as in **Figure 2-5**. The two boards are used one for the transmitter and the other for the receiver.

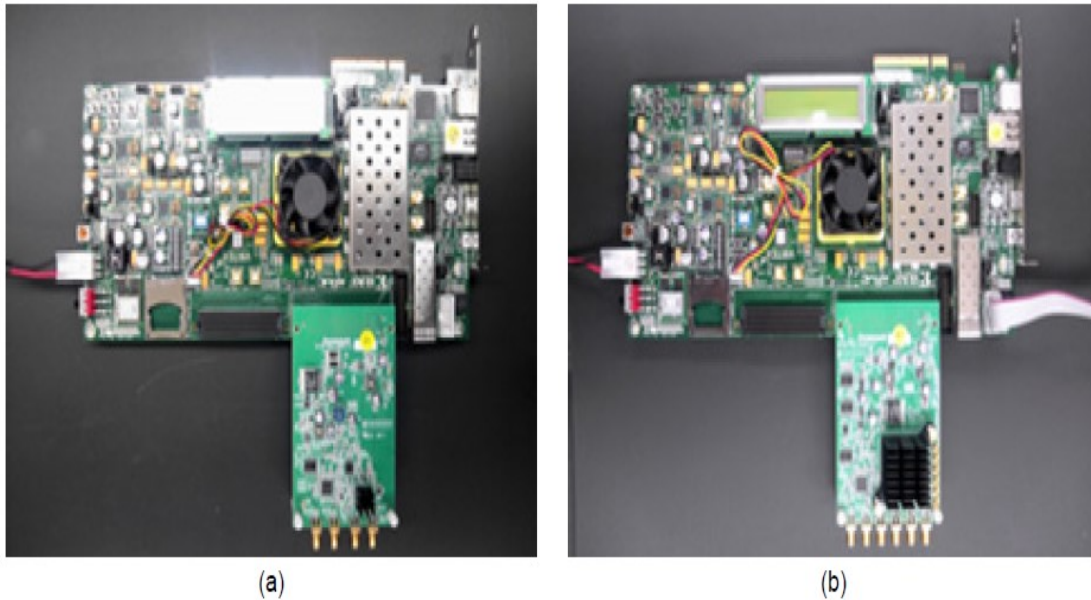


Figure 2-5 (a) FPGA based transmitter. (b) FPGA based receiver.[52]

The bit precision calculation is configured between 8 and 34 bit and the power consumed for the transceiver is shown in **Figure 2-6**. The figure displays the power of two evaluation boards, and the FPGA power is increased with bit precision, but significant increase between (2 to 18W) with different modulation types QPSk and 16QAM.

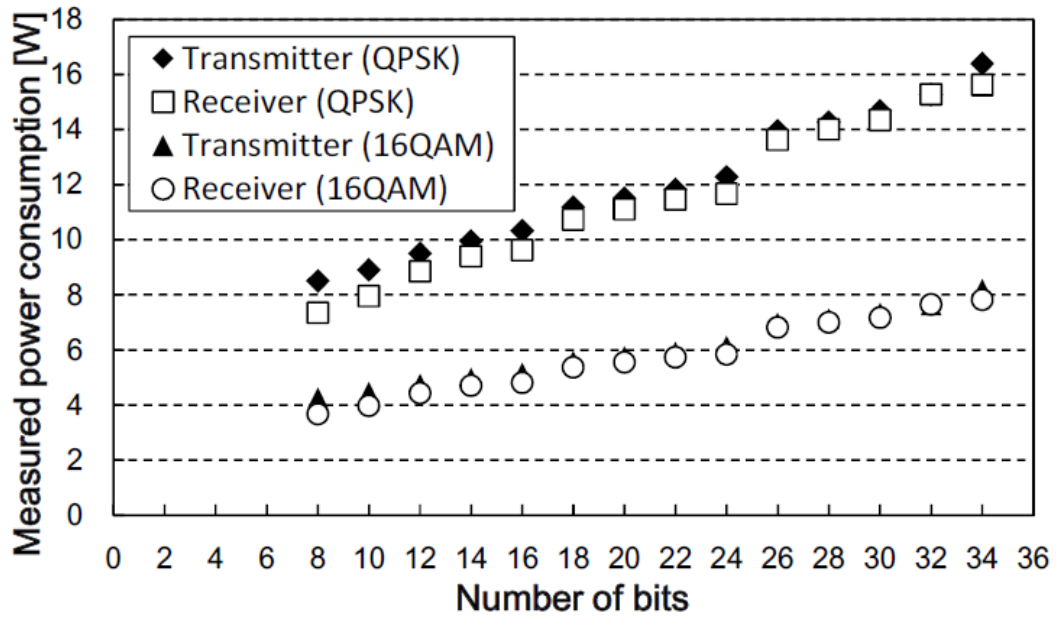


Figure 2-6 Transceiver power consumption measurement. [52]

The power consumption measurement of the transceiver in the figure above shows the power of all system but not focusing on one part of the design. In addition, the QPSK has more power consumption than 16QAM because the FPGA runs at twice the speed of the FPGA for the 16QAM.

The DSNR method uses variable precision DSP to control the number of bits used in FFT/IFFT calculations which reduces or increases the bit number to satisfy the BER and optimise the SNR [53]. However, the reduction of the bits number used in the calculation IFFT/FFT function lead to reduce the power consumption of the transceiver [7]. The downstream configuration of an energy efficient OFDM-PON (Passive Optical Network) using the dynamic SNR management technique is shown in **Figure 2-7**.

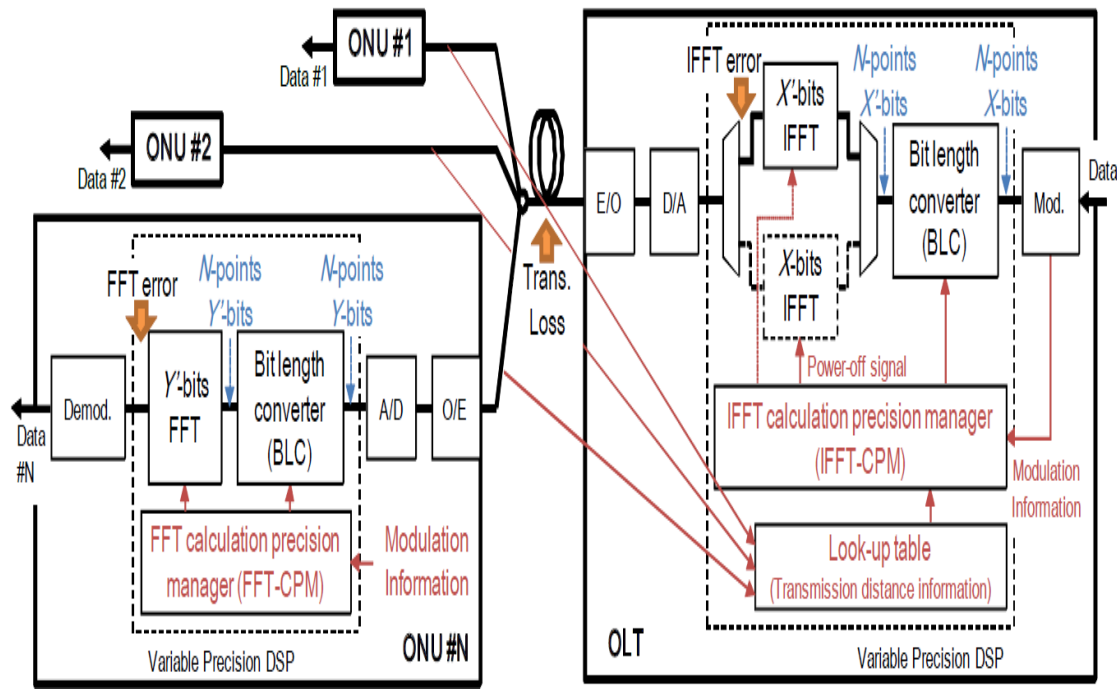


Figure 2-7 Configuration of OFDM-PON using variable precision DSP. [10]

The BLC (Bit Length Converter) used to translate the downstream signal into bits depending on subcarriers number. The BLC convert the N-Points/X-bit to N-Points/X'-bits. Where N is the number of points input to IFFT/FFT units, which depends on the number of subcarriers used in the downstream signal. X indicates the calculated number of bits and depends on IFFT CPM (Calculation Precision Manager). The CPM is dynamically optimised the bits number to satisfy the BER by referring to the look-up table and modulation techniques such as QPSK, M-QAM [52]. The look-up table contains information about the transmission distance. The IFFT is turned OFF by CPM when using a small number of bits for calculations. The relationships between transmission distance and bit length are shown in **Figure 2-8**

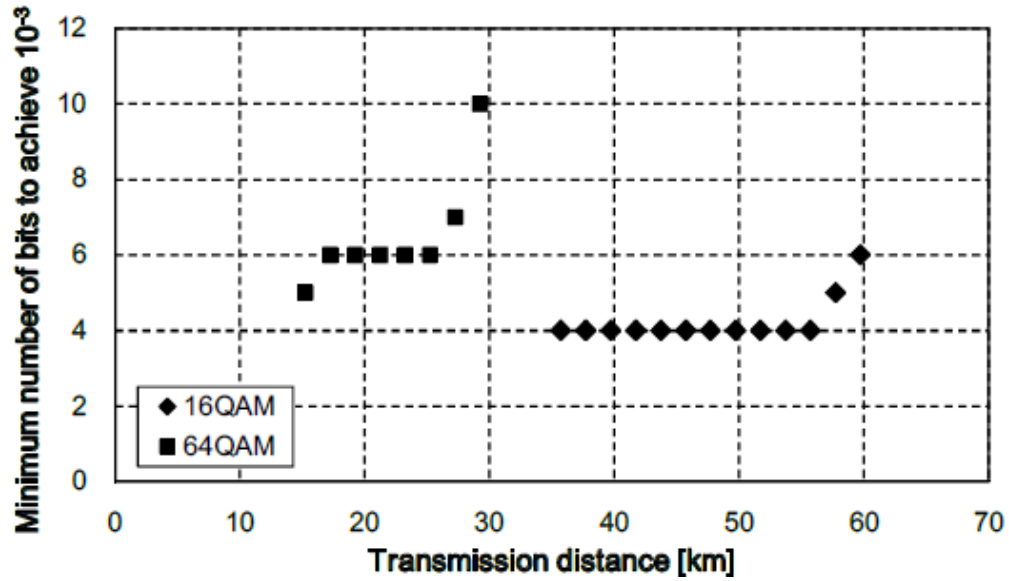


Figure 2-8 Error and transmission distance for different bit length. [10]

The simulation results in the figure above shows the relationship between the distance and the minimum number of bits needed to achieve a BER of 10^{-3} . These results indicate that calculation with a small number of bits for short distance communication. The block diagrams of the transmitter and receiver is shown in Figure 2-9.

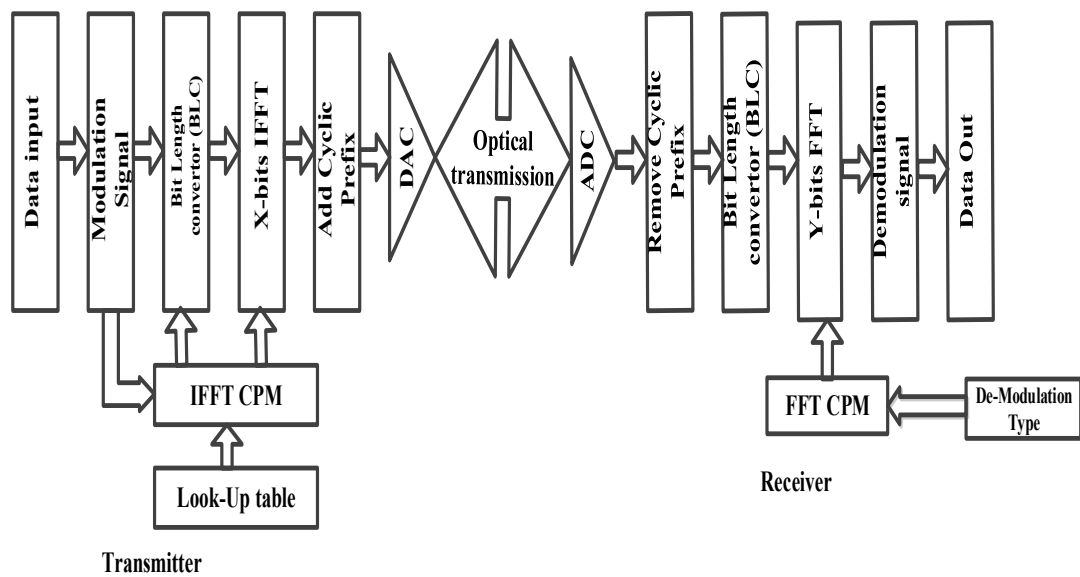


Figure 2-9 OFDM design model by DSNR.

The rounding and quantisation error depends on the calculation precision which means the number of bits used for calculation of IFFT/FFT.

The precision control is used to optimise the number of bit per subcarrier input to IFFT/FFT and select the optimised number of bit required for calculation precision to satisfy bit error rate which reduces the power consumption in different modulation format [54]. This method used two FPGA boards and focuses on transceiver total power when changing the precision of the IFFT and modulation type. The DSNR effects on the transmitted signal power and signal to noise ratio. This method is used in this research to investigate the effect of bit precision and modulation type on IFFT/FFT power consumption using one FPGA board.

2.3 Adaptive Cyclic Prefix.

The Cyclic Prefix (CP) and Guard Interval (GI) are essential techniques for OFDM systems because they are used to eliminate the effect of intersymbol interference (ISI) or intercarrier interference (ICI). The ISI is created on the transmitter side of the OFDM transceiver when the encoded subcarriers are processed in IFFT to generate OFDM symbols. When the distance between the following symbols is small, this will produce interference or overlap between OFDM symbols [55]. The solution for ISI by setting a small gap between OFDM symbols and fixed the distance between symbols. The adding CP procedure by copying the last fraction samples of each OFDM symbol in the time domain and inserted at the beginning of the same OFDM symbol as in **Figure 2-10**.

The Cyclic Prefix length increase between the OFDM symbol which produces a channel delay and increases the channel power of the transmission [56]. Moreover, the increases length of CP symbol led to reduces the bandwidth efficiency and decreases the data rate (system capacity) because the CP symbol is not carried any data that means zero bits and reduces the signal efficiency with decreases the SNR by increasing the OFDM symbols noise [11][56].

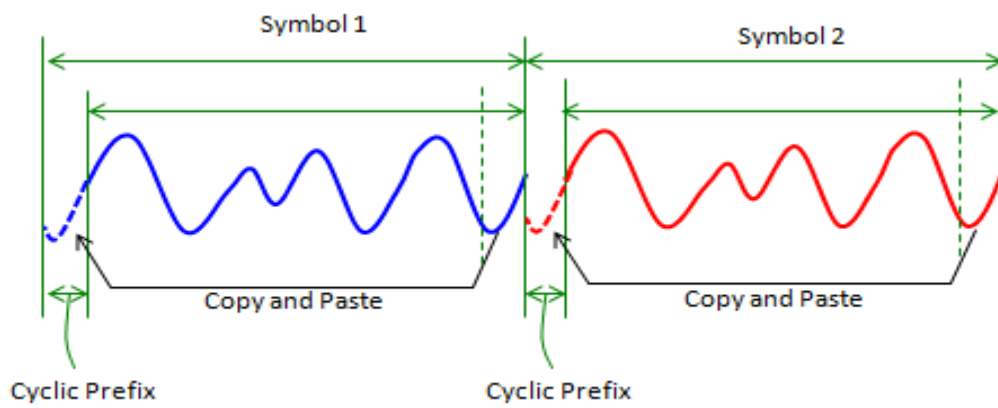


Figure 2-10 Mechanism of Cyclic Prefix

A cyclic prefix mechanism is implemented by inserting a gap between adjacent symbols and filling the gap using a CP. The equation (2.5) of OFDM CP as [56] :

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k) e^{j \frac{2\pi n k}{N}} \quad (2.5)$$

$X(k)$: Frequency domain modulated subcarriers

$x(n)$: Time-domain samples

$n = -G, \dots, 0, 1, 2, \dots, N-1$

G = CP length

N : IFFT size

K: 0,1,2,.....N-1

There are two types of CP:

- Fixed length CP type: the length is equal to the percentage of the subcarriers input for example 10% for all OFDM symbol. The CP is inserted between the OFDM symbols in the transmitter side after processing IFFT to extend the time domain period, and it is equal to the length (number of samples) between all the OFDM symbols [57][58]. The OFDM Transmitter block diagram with Cyclic Prefix location as in **Figure 2-11**.

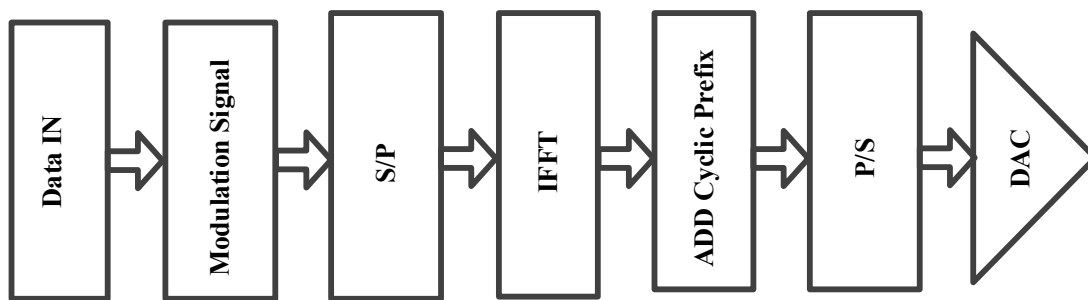


Figure 2-11 OFDM model with Cyclic Prefix.

The optimum value of the cyclic prefix is selected for the OFDM symbol which is used to reduce the effects of ISI. The fixed length CP type is not efficient because reduces data rate, increases channel delay, and increases the energy of the channel transmission.

- Another types of CP uses a variable length which is more efficient than a fixed type. The advantage of this method is to improve the data rate when compared with fixed length CP. In variable length, the optimum value of CP is selected by depends on the BER in the receiver side. In

addition, selected optimum length CP that satisfied the BER of the transmitted signal as shown in **Figure 2-12**.

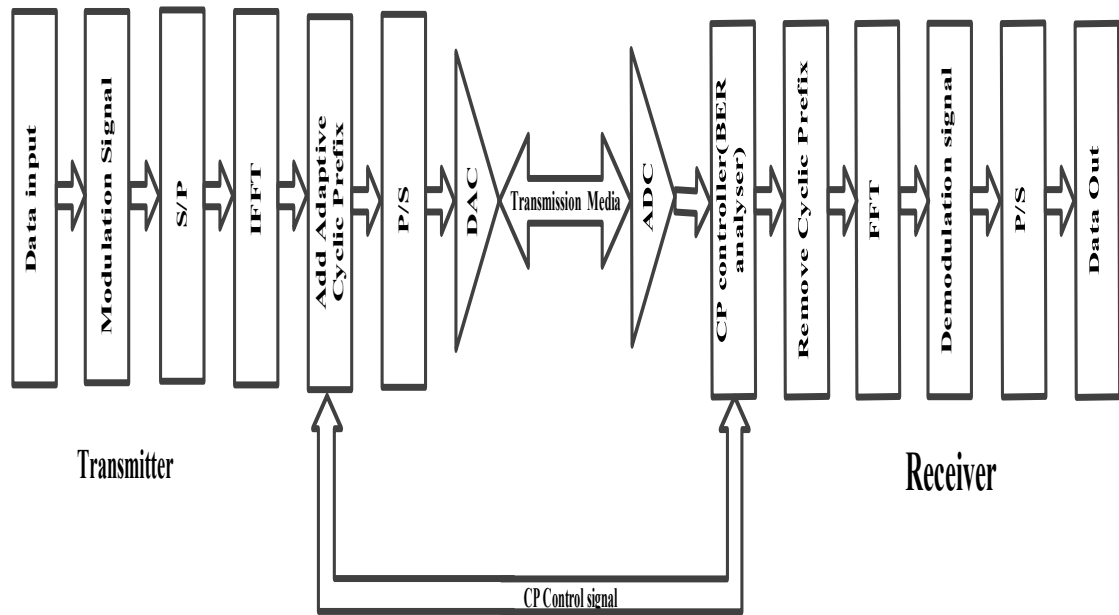


Figure 2-12 OFDM with Variable CP

This method controls the length of CP by selecting the optimum BER on the receiver side and send a feedback signal to the transmitter to select the optimum length of CP. Moreover, ACP provides a reduction in the unused bandwidth in OFDM symbols and improves the bandwidth of the transmitted signal; the result is an improvement of the transmission performance and energy.

The result compare between fixed type CP and ACP in MIMO system using an OFDM [56] is in **Figure 2-13**.

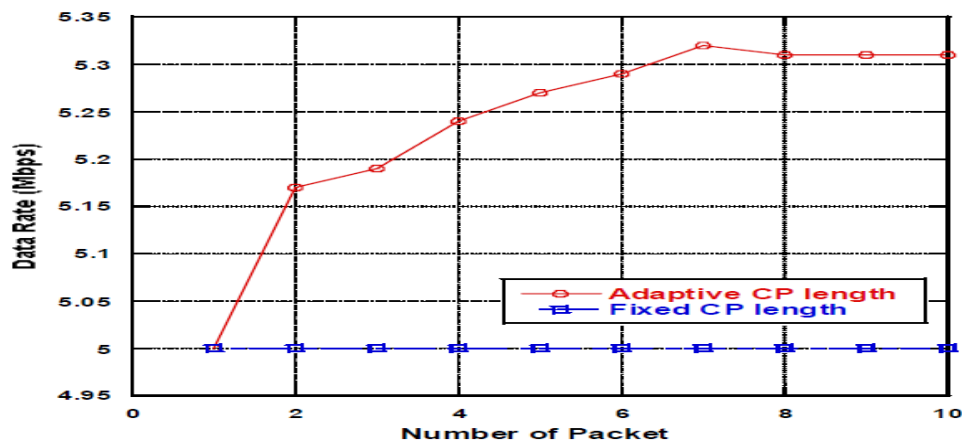


Figure 2-13 Data rate comparison between ACP and fixed CP. [56]

The figure above describes the difference between fixed CP and ACP. The Blue line is the conventional OFDM system with fixed CP, and the red line is the OFDM system with adaptive CP length. In case of using fixed CP, the data rate is not the same of using ACP. However, the OFDM system using adaptive CP length increases the data rate about 10Mbps when compared with fixed CP. The comparison in term of power loss is in **Figure 2-14**.

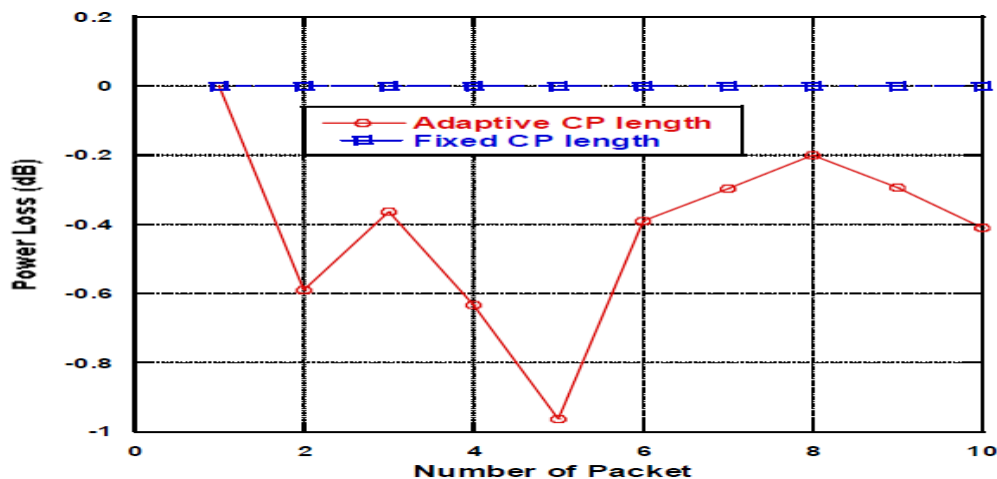


Figure 2-14 Power loss compare between CP and ACP [56]

The figure above shows that the power consumed by ACP is lower than the fixed CP used in OFDM system.

2.4 Adaptive Loading Algorithm

The adaptive algorithm has been used in the implementation of Optical OFDM to improve the transmission performance [59]. Applied different loading algorithms on the subcarrier to generate the OFDM symbol which produces a full usage of the orthogonality between different subcarriers within the Optical-OFDM symbol [60]. In addition, improves the system flexibility and transmission performance and the energy of each carrier in optical OFDM can achieve by increasing the utilisation of each sub-carrier by applying various adaptive loading algorithms [60]. The block diagram shows the interaction of the three ALA methods equipped with an OFDM transceiver is shown in **Figure 2-15**.

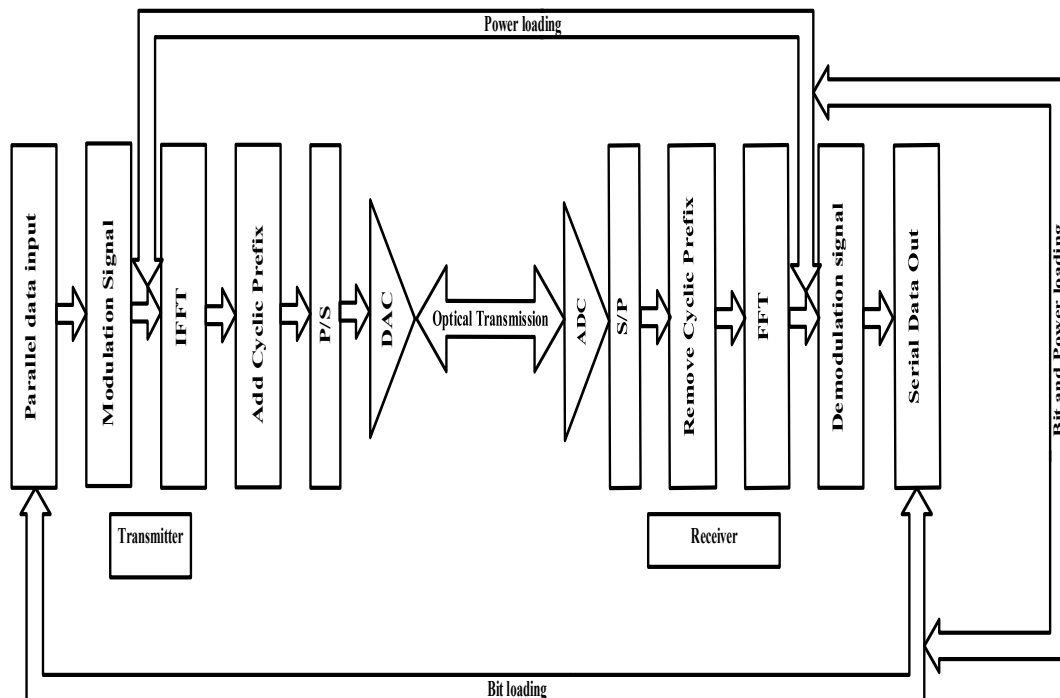


Figure 2-15 Adaptive loading algorithm techniques

There are three types of adaptive algorithms as described below:

1. Bit Loading (BL) algorithm: the same power for the subcarrier with a different modulation format applied [61]. This algorithm manages the number of bits per subcarrier by depends on the modulation format level to optimise BER [62]. The BL algorithm negotiates between transmitter and receiver in the frequency domain before modulation in the transmitter side to apply different modulation format, and after demodulation in the receiver to check error [63]. In addition, the Optical OFDM system uses BL by enables the variation of the signal modulation format level for each subcarrier including equal power for all subcarriers. This technique reduces the total energy per bit when compared with BPL [13][64].
2. PL (Power Loading) algorithm manipulates the electrical subcarriers power but using the same modulation format for all sub-carriers with high order modulation format [60]. This method consumes significant signal power by depends on the BER in the receiver side.
3. BPL (Bit Power Loading) algorithm adjusts both modulation and power for each subcarrier individually. This algorithm combines both aspects of the two algorithms above [59]. The best bit rate transmission can be achieved with the BPL algorithm but it suffers from high computational complexity in a transceiver, and the transmission performance is usually best for BPL and worse for PL [64].

The comparisons between the three adaptive algorithms above are described in Figure 2-16, Figure 2-17, Figure 2-18 :

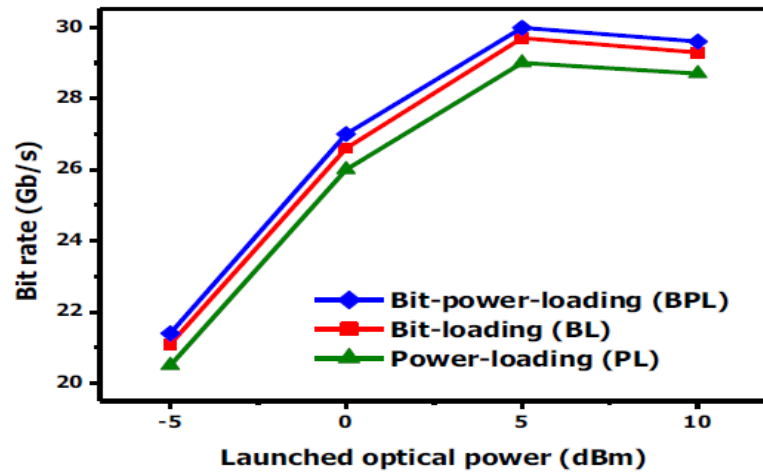


Figure 2-16 Signal bit rate versus launched optical power over a 40km SMF link for PL, BL and BPL. [59]

It is shown, from Figure 2-16 above that a small signal capacity difference of up to about 7% is observed between the BPL (best) and PL (worst) algorithms. It should be noted that the performance of BL is very close to the BPL over the entire range of launch optical power and transmission distance

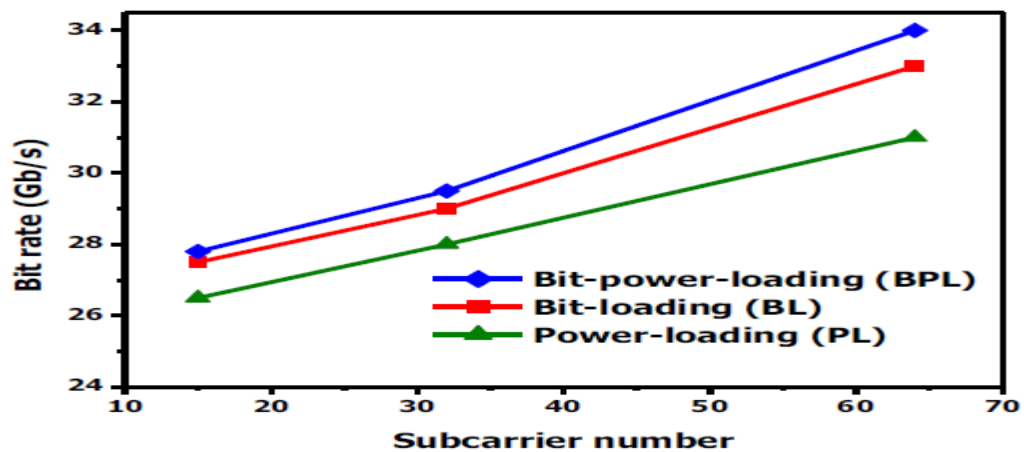


Figure 2-17 Signal bit rate versus a number of subcarriers over a 40km SMF link for PL, BL and BPL. [59]

Figure 2-17 shows that the signal capacity difference between BPL (best) and PL (worst) algorithms, as well as the difference between BL and PL (worst), increases when a large number of subcarriers are employed. In particular, the BPL-PL (BL-PL) signal capacity difference increases up to about 10% (7%) when 64 subcarriers are employed, while for the case when 15 and 32 subcarriers are considered, the signal capacity difference is at only about 5% (3.5%).

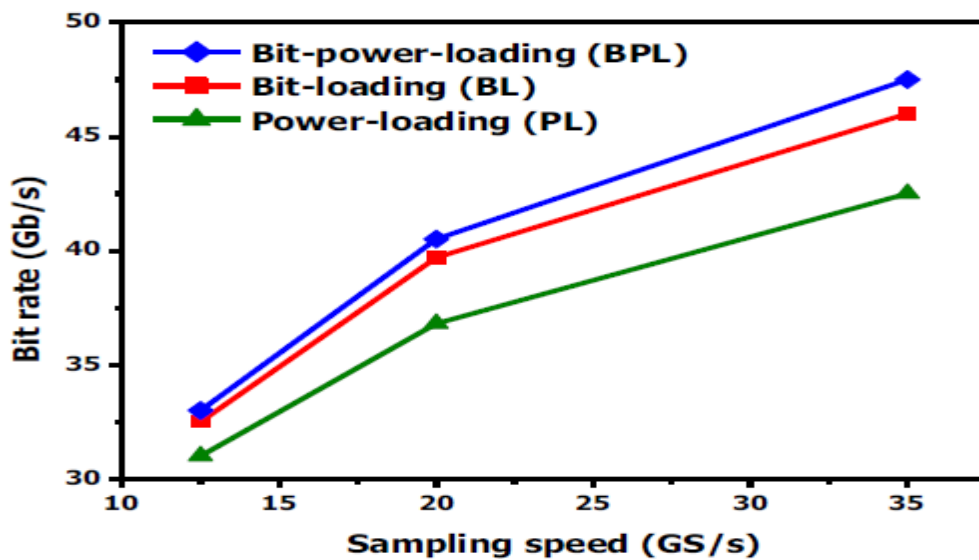


Figure 2-18 Signal bit rate versus sampling speed, employing 64 subcarriers over a 40km SMF link for PL, BL and BPL.[59]

In Figure 2-18 the signal capacity versus sampling speed is depicted, revealing that for high sampling speed of 35 GS/s, the signal capacity difference between BPL-PL (BL-PL) is about 12.4% (8.3%). On the other hand, for low sampling speeds such as 12.5 GS/s, the BPL-PL (BL-PL) signal capacity difference drops to about 7% (4.8%).

2.5 Hermitian Symmetry

It is a particular arrangement subcarriers input to obtain the real-valued time-domain signal from IFFT when symmetric complex [65]. The purpose is usually the channel: if the signal is transmitted over a low-pass channel without additional radio-frequency up-conversion (which requires an oscillator at the transmitter and a local oscillator at the receiver) [66][39] the transmit signal must be real-valued. The equations of the Hermitian signal is described as follows [67].

The Fourier direct transform equations as

$$X(w)F\{x(n)\} = \sum_{n=-\infty}^{\infty} x(n)e^{-i\omega n} \quad (2.6)$$

The inverse transform equations

$$x(n) = F^{-1}\{X(w)\} = \frac{1}{2\pi} \int_{2\pi} X(w)e^{j\omega n} dw \quad (2.7)$$

The signal is represented as $x(n)$, and it is transformed $X(w)$ which complex-valued function. Then the signal is expressed as

$$x(n) = x_R(n) + jx_I(n) \quad (2.8)$$

$$X(w) = X_R(w) + jX_I(w) \quad (2.9)$$

Submit eq. (2.8) and $e^{-i\omega} = \cos(w) - j\sin(w)$ into (2.6) and spared real and imaginary part

$$X_R(w) = \sum_{n=-\infty}^{\infty} [x_R(n) \cos wn + x_I(n) \sin wn] \quad (2.10)$$

$$X_I(w) = -\sum_{n=-\infty}^{\infty} [x_R(n) \sin wn - x_I(n) \cos wn] \quad (2.11)$$

When submitting equation (2.10) and $e^{j\omega} = \cos(\omega) + j\sin(\omega)$ to equation (2.7) the equation obtain is shown below

$$x_R(n) = \frac{1}{2\pi} \int_{2\pi} [X_R(\omega) \cos \omega n - X_I(\omega) \sin \omega n] d\omega \quad (2.12)$$

$$x_I(n) = \frac{1}{2\pi} \int_{2\pi} [X_R(\omega) \sin \omega n + X_I(\omega) \cos \omega n] d\omega \quad (2.13)$$

The real signal is expressed by $x(n)$ is real then $x_R(n)=x(n)$ and $x_I(n)=0$. The equations (2.10) re-written as in equations below

$$X_R(\omega) = \sum_{n=-\infty}^{\infty} x_R(n) \cos \omega n \quad (2.14)$$

$$X_I(\omega) = -\sum_{n=-\infty}^{\infty} x_R(n) \sin \omega n \quad (2.15)$$

Since $\cos(-\omega n) = \cos \omega n$ and $\sin(-\omega n) = -\sin \omega n$ then the two equations (2.14) and (2.15) re-written as follows

$$X_R(-\omega) = X_R(\omega) \text{ for even } (2.16)$$

$$X_I(-\omega) = -X_I(\omega) \text{ for odd } (2.17)$$

The two equations (2.16) and (2.17) combined into the single equation the result in equation (2.18)

$$X^*(\omega) = X(-\omega) \quad (2.18)$$

The (2.18) represents the spectrum of the real signal using Hermitian symmetry.

2.6 Complex value IFFT.

The complex type IFFT is referred to as the output symbol generated from the IFFT block when the input is two parts (real and imaginary) but not symmetric [68]. Therefore, the output symbol divided into two-part, real and imaginary, after DSP processing calculation including additions and multiplications inside IFFT [69].

$$X(K) = \sum_{n=0}^{N-1} X(n)W_N^{nK} \quad K=0,1,2,\dots,N-1 \quad (2.19)$$

Where: $W_N = e^{j(\frac{2\pi}{N})}$ is a twiddle factor.

$X(n)$ is complex input subcarriers [70]

The computational complexity of IFFT/FFT is calculated [71] as in the equation (2.20).

$$\text{Computational complexity} = N * \log_2 N \quad (2.20)$$

The (log) base assign to the radix order number and N means the length of IFFT/FFT. Therefore, the equations in this section used Radix-2 pipeline IFFT [72].

The number of Complex addition [73] of N point IFFT is

$$\text{Complex additions} = N \log_2 N \quad (2.21)$$

The number of Complex Multiplication as in the equation (2.22)

$$\text{Complex multiplications} = \frac{N}{2} \log_2 N \quad (2.22)$$

This method is used widely in conventional OFDM to generate the OFDM symbol.

2.7 Recursive DFT

The DFT/IDFT have widely been applied in DSP applications such as communication system. The parallel architecture of several DFT algorithm increased the control complexity and complicated the data bandwidth of circuit models [74]. The pipeline architecture normally uses 2^n points of DFT also the radix 8 is a three steps algorithm used to compute 8192 points frame size.

There are several methods used to implement the RDFT which it used to compute the DFT/IDFT with lower mathematical multiplication, Read Only Memory, more area efficient than an algorithm based on the pipeline parallel processing, and increase the data throughput per transform. The Goetzl's algorithm [75] uses in the implementation of the RDFT. The advantage of this algorithm can be realised without an input buffer; input sequence can be fed by serial-in/ serial-out and dynamically cope with variable frame sizes. The RDFT does not require a large amount of RAM for storing temporal data and enables individual DFT results instead of computing all N-point DFTs [76]. The new flow chart of RDFT structure is shown in **Figure 2-19**

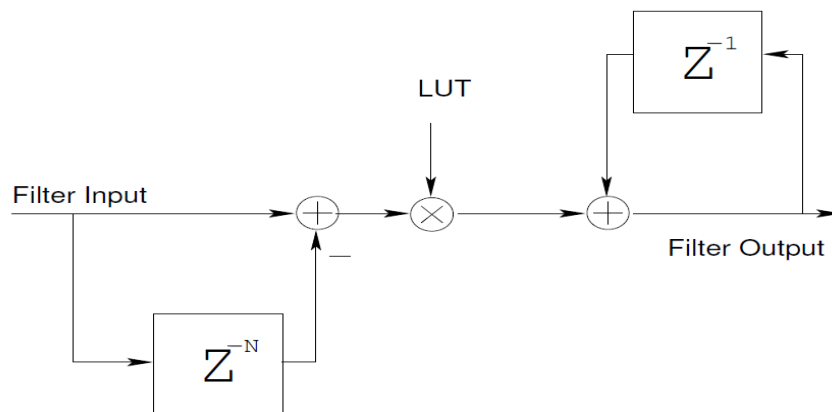


Figure 2-19 RDFT structure. [77]

This algorithm needs a three computational cycle for whole DFT computations to compute the RDFT. This algorithm is not depends on N length and depends on constant. The mathematical computation of RDFT includes three operations which two addition and one multiplication. The number of $e^{-j2\pi nk/N}$ are powers of the N^{th} root of unity and normaly stored in a look up table. The multiplication occurs because of the exponential and the constant x_n in the equation of RDFT[78].

$$H_k = \sum_{n=a-(N-1)}^a x_n e^{-j2\pi nk/N} \quad (2.23)$$

The current value of DFT is represented by H_k ; the current sample is x_a . The Recursive DFT/IDFT formulas reduce the needless requirement for an additional multiplexer in hardware implementation. In addition; this type is very fast, low power, but need multi RDFT to generate the OFDM symbol.

Yang and Chen [79] uses the two hardware structures to reduce the cost of implementation DFT computation but the critical period of computational cycles and computation were larger than those in the previous work. Van and Yang [80], [81] proposed a new method to reduces the limitations on performance which is high performance and power efficient for (VLSI) algorithm and architecture.

The Clenshaw's recurrence relation uses as a recursive solution to reduce the computational implementation complexity of DFT [82]. This method formulas to drive a simple, regular and locally connected linear array architecture for systolic implementation of the DFT. The RDFT implemented by this method reduces the complexity and have driven a fully pipelined linear systolic array for computational DFT.

The recursive DFT with low cost, fast computational, power-efficient, and reconfigurable is implemented with Prime Factor Algorithm (PFA)[83], and the Chinese Remainder Theorem (CRT) [84]. This scheme is based on the technique of register splitting and the resource-sharing. This combination type is a better performance, hardware resources, coefficient requirement, and computational complexity when compared with the previous existing RDFT algorithm [85]. This algorithm uses fewer computational cycles, decrease the computational complexities of additions and multiplications, and lower coefficient memories. This algorithm is suitable for VLSI realisation for variable length DFT. The application of using RDFT in Commensal Radar which is used the transform in computing the Doppler processing for computing amplitude range data instead of using FFT [86].

The HDFT algorithm computes the DFT by incorporating the successive DFT outputs with arbitrary-time hop L . the increasing number of time hops will be increasing the calculation complexity and hardware costs. This is the major reason to develop the rHDFT algorithms. The new DFT algorithm, called Recursive Hoping DFT (rHDFT) used to reduce the complexity, hardware cost in implementation when compared with HDFT [87]. The (rHDFT) reduces the complexity of the algorithm, hardware cost implementations, and mapped into a hardware accelerator.

2.8 Summary

This chapter has discussed the previous methods which focused on complexity, processing and power of the signal that is affected by OFDM modulation.

1. The Fast-OFDM is used to reduce the complexity of the processing in the OFDM and generate the real OFDM symbol. This method uses slow transform type such as DCT/IDCT, but the fast transform type uses IFFT/FFT with Hermitian symmetry to produce real value OFDM symbol.
2. This chapter discussed bit precision by DSNR which is used to control the bit precision of the IFFT/FFT calculation. It effects on BER and the accuracy of the OFDM symbol and the power consumption of the OFDM transceiver system. In DSNR experiment uses two FPGA board (transmitter and receiver) for implementation of the DSNR.
3. The ACP discusses CP length on the energy of the transmission channel. The variable length called ACP improve the channel efficiency by reducing the delay due to fixed type CP. The CP length increase led to increasing OFDM symbol length which increases the delay of the channel and increases transmission power. The result compared to fixed and variable length CP has discussed.

4. The background analysis of the method used to generate the real value signal was discussed such as the Hermitian symmetry method used to generate a Real-Value OFDM. In addition, the Complex value IFFT used in this thesis.
5. Reviewing methods uses to compute the recursive DFT which is low power, low memory, high-speed data processing and implemented in parallel processing for individual DFT.
6. The effect on OFDM power consumption reviewed method has published in [88]



Chapter

Three

CHAPTER 3

3 SOFTWARE PLATFORM AND TOOLS USED

The FPGA Power consumption has become a critical issue in the development of an embedded system which depends on a specific parameter at high-level FPGA design [89]. The demands on FPGA power measurement tools increased very rapidly during last years because of increasing the application of power saving. The area and cost of the embedded system are essential factors for the system designer to provide an accurate estimation of the FPGA resources [90].

In addition, design modelling with high-level tools make it possible to synthesise high-performance FPGA design from the Simulink model. In the past, the power estimation of the hardware resources suffered from inaccuracy, slowness, and high complexity, which limited their implementation [91][36]. The implementation uses the Xilinx system generator which combines the Matlab and Xilinx Simulink library to generate a power report of the design by the power estimator tools [35]. The following section discusses the design method and the procedure of power report generation for the OFDM design.

3.1 ISE Design Suite.

The Xilinx Integrated Synthesis Environment (ISE) is an FPGA/CPLD design environment developed by Xilinx. It uses FPGA embedded system to programming with specific editions such as ISE Embedded edition, ISE system edition, and WebPack edition [38]. The Embedded edition type uses

by a researcher must include a license and the system edition uses university or group license.

The WebPack edition is free to use and has limited tools included. Xilinx developed ISE Design Suite for synthesis and analysis of HDL designs which enable the designer to compile their design, perform timing analysis, configure the target device with a programmer, and examine the real-time operation of the target device.

3.2 System Generator Design Environment

The System Generator is developed by Xilinx uses MathWorks Environment based on Simulink for model design. The System Generator includes a DSP design tools help the designer to design the Simulink model inside MathWorks environments [92]. These tools help the designer to develop high-performance DSP system for Xilinx FPGA. The design is simulated using MATLAB code, Simulink blocks, and Xilinx library.

The Xilinx tools extend the Simulink to provide a modelling environment which is compatible with hardware design. The System Generator offers high-level tools which automatically compile the model into an FPGA. The system generator tools provide access to FPGA resources through low-level structure tools to get high efficient FPGA design [93].

Xilinx System Generator will automatically generate synthesizable HDL (Hardware Description Language) code by using specialised tools [94]. These tools will synthesise the model and then implement it on Xilinx FPGA hardware. The synthesis is a construction level of the logic gate for the design model from the high-level design.

The design can execute faster in computing program, allows higher logic density, reduces project time, and cost. The System Generator is not meant to replace HDL languages but to make it possible to focus on the critical paths. The model design is more efficient through using IP cores that provide a range of arithmetic operations for various complex functions [36]. The design of the system by the logic gate with IP core which is an efficient FPGA design that includes a complex function such as IFFT/FFT. The System generator hardware Co-Simulation interface allows simulating the hardware under Simulink under an environment of Matlab and Simulink to produce the best data analysis and visualisation [95].

3.3 Target device selection.

Power reduction has become a primary concern for the FPGA developer because the higher-speed circuit will consume significant electrical power. Therefore, the challenge for the FPGA developer has improved the performance because of the power budget. Xilinx has found a solution by developing a 28nm Xilinx FPGA which is used in many FPGA applications. The Xilinx Kintex-7 FPGA family is designed for balanced power, performance and providing a high-end feature such as extensive DSP resources, integrated IP, and cutting-edge transceivers [96].

The selection of the Xilinx Kintex-7 instead of a different FPGA such as Altera by depends on the comparison between the manufacturing firm of FPGA. The Xilinx FPGA embedded system is significant efficient power consumption than the Altera [97]. The Xilinx 7 series family of Kintex-7 offer low power consumption when compared with Altera FPGA.

The practical experiment compares between Xilinx and Altra regarding power consumption which is used in communication application [98][96]. The result has Xilinx offer high-performance, low power consumption per Watt with cell fabricated 28nm FPGA. This type of FPGA provides optimisation system power, thermal and reliability requirement. Moreover, gives an accurate estimation power to support the design and low-cost power supply with thermal management which will change late in the design cycle [99].

3.4 System Generator and Kintex-7 Development Kit interface.

The Simulink Xilinx System Generator supports the integration between 4DSP daughter card and the Kintex-7 based board [100]. The integration is used to simulate the interfacing between the development kit and the real world analogue data through the FMC150 data converter [101]. The Simulink plugin file provided by Avnet as a compressed zip file supports the interfacing and attaches to the board which is installed separately in Xilinx ISE14.7. The ISE14.7 System Generator uses the plug-in installation file which modifies the gateway I/O to support the DAC /ADC by applying the following command in the MathWorks System Generator command window

```
>> xllInstallPlugin('kintex_7_dsp_kit_plugin_14_7')
```

The DAC checkbox found in Gateway-OUT (Drive DAC input) is shown in **Figure 3-1** this Simulink block simulates the FMC150 [102] by using System generator MathWorks Simulink.

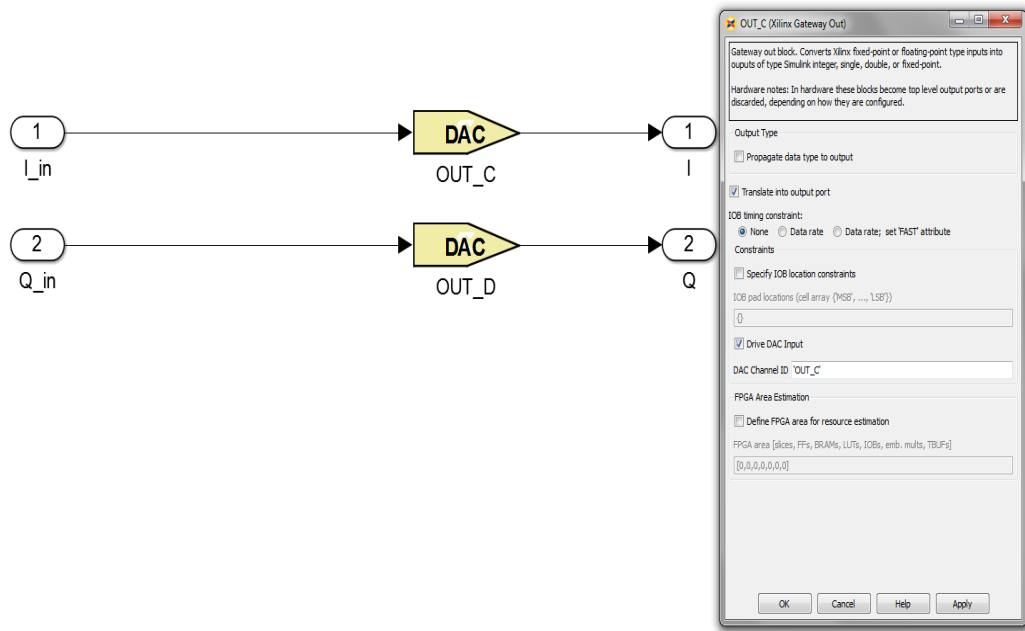


Figure 3-1 SysGen Math Works Simulink DAC block

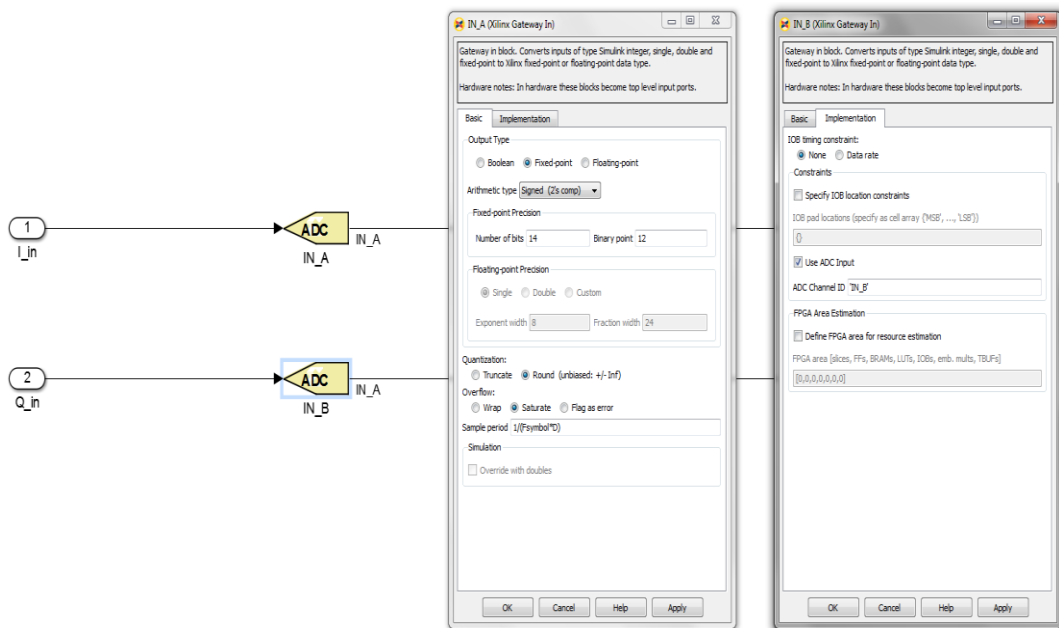


Figure 3-2 System generator ADC Simulink block

The ADC Simulation with the setting is described in **Figure 3-2**. In the setting, there is an option (Use ADC input) to activate the gateway port to ADC port and define the name of ADC. In addition, the settings page of the ADC/DAC block includes the data type input (word length) and the sampling period.

3.5 XPower Analyzer (XPA)

Xilinx provides interactive graphical tools used in FPGA power analysis. The XPA is used with the system generator software to perform FPGA power analysis for the design [103]. The XPA gives the power consumption information of the design, so the designer manages the implementation according to the power report and finds the weak path. The following functions are performed by the power analysis tools [104]:

- 1- Report thermal information (junction temperature).
- 2- Analyse power consumption for Xilinx® FPGA.
- 3- Report static and dynamic power for the different voltage supplies.
- 4- Validate the result accuracy of the estimation given in the XPower Estimator Spreadsheet.
- 5- Analyse supply voltage power by hierarchical power reporting.
- 6- Examine the data for the FPGA areas where power is reduced.
- 7- Generate design power consumption reports and add them to the overall project documentation.

3.6 XPower Estimator

The Xilinx Power Estimator uses Excel spreadsheet tools in the pre-design and implementation phases of the project which is supported by Xilinx [105]. XPE assists with architecture evaluation, device selection, appropriate power supply components and thermal management components for the application design. The specification of the FPGA product design such as power and cooling must be identified early in the design cycle and in most cases before the FPGA logic design [106].

The advantage of this method is to help the designer understand the design product power. The power estimation is performed at any time during of the design cycle uses Xilinx Power Estimator (XPE).

There are seven important steps used to estimate the power consumption of the Xilinx design by Excel spreadsheet which is summarized in the following [107] :

1. Obtain the latest version of the Xilinx Power Estimator for the selected target device.
2. Complete the Device information on the Summary tab.
3. Complete the Thermal Information on the Summary tab.
4. Set worst-case voltages for all supplies.
5. Enter clock and resource information.
6. Set the toggle and connectivity parameters.
7. Analyze the results.

In most cases, the FPGA design is not complete or sometimes not even started at this stage. Therefore, it will be easy to understand the FPGA power consumption such as design consumption power and thermal characteristics.

The easy way to understand the power estimation of the simulated design is by exporting the simulation file from the power report generated in the analysis stage [108]. This file is imported to an Excel spreadsheet which includes all information about the design. The spreadsheet can display as a graph the junction temperature and the on-chip power by the function of all components as a temperature colour and supply voltage power.

The graph in the spreadsheet uses the default setting without modification from the user. The spreadsheet file can be used to study the effect of the junction, environment, and the board layer temperature on the power consumption after modification by the user. In addition, the supply voltage sources, clocking frequency, heatsink type effects on FPGA power which is modified for worst cases.

The power change dramatically by depend on clocks and data input into the chip. The thermal and power can make FPGA work out of specification which means not operate at the expected performance and add extra cost with more complexity.

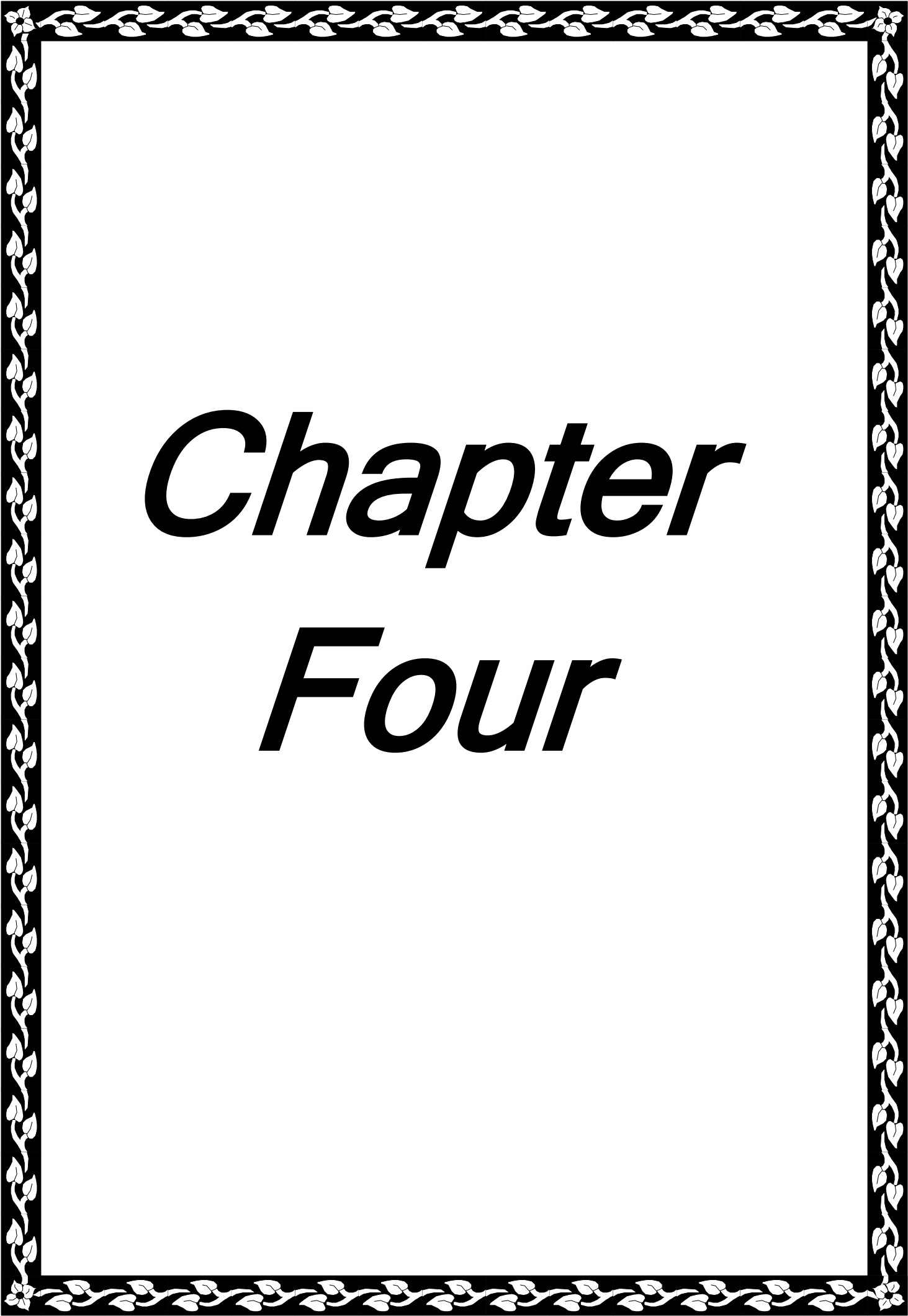
This section included some features not implemented in this thesis and expected to implement in the future work.

3.7 Summary.

This chapter has discussed the software and hardware used in the implementation stage of the OFDM model used in this thesis. The description included the method and software tools used to find the FPGA power consumption report for each part of the design especially the IFFT/FFT. This chapter includes the Xilinx System Generator interfacing with the Mathworks environment. The Simulink block interfacing benefit has been used to build OFDM model and generate the power report. The selecting Xilinx Kintex-7 hardware component by comparing power budget between two FPGA companies Altera and Xilinx which is led to choose the Xilinx FPGA in this thesis to estimate and analyse power consumption. This type of hardware including high-speed analogue DAC/ADC from 4DSP to interface the hardware with the real outside world.

The Excel spreadsheet explained in this chapter used for power consumption estimation. The researched discussion includes the step of estimation power consumption and imports the simulation file from power report. The spreadsheet features used to estimate the power consumption was discussed in this chapter for default setting and worst case modified by the user.

This chapter has used an introduction to the implementation of the OFDM model used in the next chapter to estimate power consumption of IFFT/FFT.

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Chapter

Four

CHAPTER 4

4 IMPLEMENTATION OF THE OFDM TRANSCEIVER MODEL

This chapter has discussed the OFDM system description including a block diagram and the basic parameter setting of the OFDM design. In addition, discussed the proposed real value IFFT use in OFDM implementation, and the type of input subcarriers feed IFFT to generate real value OFDM symbols. The implementation procedure of the two OFDM system transceiver real and complex uses Xilinx System Generator Simulink software. The FPGA power report focuses on one part of the OFDM design model IFFT/FFT. In this chapter has investigated the researched parameters which are affected by the FPGA power consumption of IFFT/FFT on the OFDM design. The rest of this chapter has analysed the researched parameters setting effect on FPGA power consumption of IFFT/FFT. The result compares between the two models real and complex value IFFT used in OFDM which implemented in System Generator Simulink by using FPGA evaluation board Kintex-7. In addition, The subcarrier type uses QPSK and 16QAM with a different setting which is generated by Matlab code and imported to System Generator design.

4.1 System description

The OFDM model is built by Xilinx System Generator ISE 14.7 Simulink block with MatlabR2012b. The purpose of using this type of computer software is because it includes tools which can simulate the hardware and DAC/ADC.

CHAPTER FOUR ***IMPLEMENTATION OF THE OFDM TRANSCEIVER MODEL***

In addition, the Xilinx system generator can generate the power report of the simulated design. The OFDM model design components use the Matlab code and Xilinx Simulink libraries blocks such as IP core IFFT/FFT, RAM, ROM, Gateway I/O, and DAC/ADC.

The first step of the OFDM implementation procedure is to generate the encoded subcarriers by using the Matlab code. The result is exported to the Simulink Xilinx System Generator to feed the IFFT. In the Simulink side, the processing of the incoming subcarriers occurs inside of the IFFT to generate the OFDM symbols.

The OFDM symbols generated are transmitted as an analogue signal by converting the digital symbol to analogue. The OFDM symbol is converted to analogue in the transmitter side and then to the digital format in the receiver using DAC/ADC which is the special tool from Xilinx System Generator ISE14.7. The received OFDM symbols are De-Orthogonal by FFT and send to Matlab code for demodulation and recovering the original signal.

The conversion advantage is to make accessible adaptation our design in optical communication by adding an optical modulator and demodulator between DAC/ADC which would make this model compatible with optical network communications. The simulation of DAC/ADC was described in the previous chapter by interfacing Xilinx gateway through Matlab Simulink. In the next step, a power report is generated to discover the effect of various parameters on IFFT/FFT. These parameters are divided into output type from IFFT (real and complex), phase factor bit precision inside IFFT/FFT, subcarriers modulation types feed IFFT, IFFT/FFT length, subcarriers word length, and the Cyclic Prefix length effect on the IFFT/FFT IP core.

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Finally, compare the result for the various parameters above between each other by using a Simulink block from Xilinx for the two models built. The flow chart of the OFDM design model is shown in *Figure 4-1*

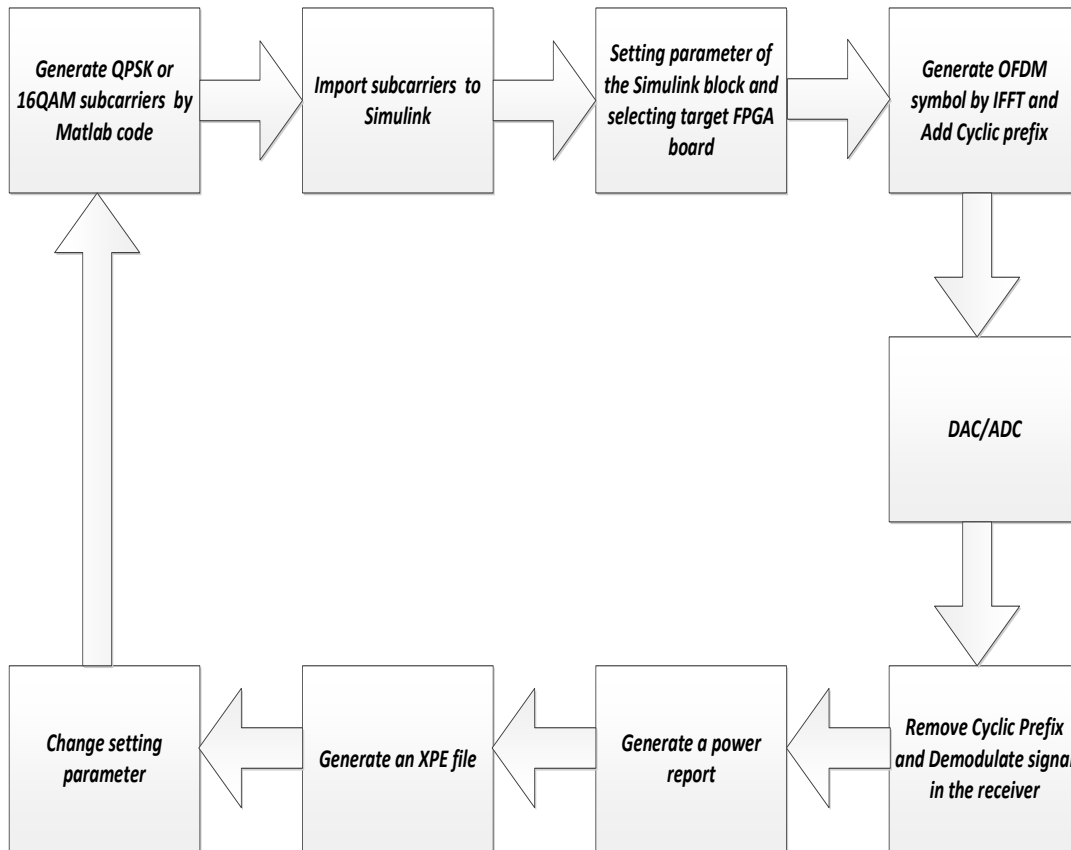


Figure 4-1 Flow chart of the OFDM model with power report

The block diagram above shows the main components of the OFDM design model used in this thesis. The first step of the OFDM design by generating an encoded data subcarriers uses Matlab code which is encoded as QPSK or 16QAM and represented in the first block. These subcarriers are imported to System generator Simulink and loaded into ROM with a specific length equal to IFFT length. The encoded subcarriers are arranged as normal input feed IFFT to generate a complex value OFDM or complex conjugate and double up the input feed IFFT to generate a real value OFDM.

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The subcarriers are feed to the IFFT which generates the OFDM symbol with a specific length of CP.

However, the output parallel symbol is converted to a serial signal and feed the Simulink block DAC/ADC. The received signal is converted from serial to parallel format, removing CP, and OFDM symbol is demodulated by the same modulation type in the transmitter.

Finally, generate a power report of the OFDM model design described above and design by Simulink Xilinx System Generator. The power report includes the power consumption for each block of the design and focuses on the IFFT/FFT Simulink block part. Moreover, the various sets of the parameters are applied which is described in previous to this design and re-execute the program to generate a power report for each design with a specific setting.

The parameters apply such as various bit precision start from 8-32 bits and generate the power report for each bit precision calculation and display the result of IFFT/FFT power. The same procedure described above is applied to the other parameters such as CP, FFT/IFFT size, subcarriers sampling frequency, subcarriers modulation, word length, and complex and real IFFT.

There are two OFDM models used to compare the power consumption which is focused on one part IFFT/FFT. The first model generates a complex output from IFFT called complex value OFDM. The second OFDM model uses a complex conjugated for the imaginary part with two location set to zero and doubles up the real part to feed the IFFT. The resulting output from IFFT called real value OFDM symbol. The power report is generated for both model above with various parameters applied and the results compared as described in this chapter.

4.2 Proposed Real value IFFT

Today most application of digital world has used a real value signal for the transmission, and the IFFT/FFT computation plays an important role for the generating a real-valued signal which is referred to real value IFFT [71]. The most application today uses real physical signals such as biomedical signals and Optical OFDM [68]. The procedure of generating a real value output from IFFT by arranging the symmetric input subcarriers feed to the IFFT as in Hermitian. The analyses of the real value IFFT is discussed and analysed in ref [109] which discovered in 1987 but not implemented in OFDM. Therefore, the subcarriers feed to IFFT is divided into two parts real and complex. The real parts input feed to IFFT is double up input. The complex part input to the IFFT is divided into two parts with conjugated to each other, and the two location is set to zero, so the output is a real value. The real IFFT is lower complex than the Complex IFFT [110].

The equation below represents the proposed design model of the real IFFT is in equation (4.1)

$$X[n] = \frac{1}{N} \left\{ \text{Re}(X(0)) + \sum_{k=1}^{\frac{N}{2}-1} X(k) e^{\frac{j2\pi nk}{N}} + \text{Re} \left(X \left(\frac{N}{2} \right) \right) + \sum_{k=\frac{N}{2}+1}^{N-1} X(N-k)^* e^{\frac{j2\pi nk}{N}} \right\} \quad (4.1)$$

Where: $n=0, 1, \dots, N-1$

N : length of IFFT

CHAPTER FOUR *IMPLEMETATION OF THE OFDM TRANSCEIVER MODEL*

The $X(k)$ is complex (real and imaginary) which is the subcarriers input, but there is two location of imaginary input has been set to zero which is shown in equation (4.2).

$$X(0 \text{ and } N/2) = 0 \quad (4.2)$$

The resulting output from IFFT is real only, and the imaginary part approximately set to zero. In this type of IFFT, the two input part is used to obtain one output real but double up the data sequence output for the OFDM symbol. The output from IFFT is double up data sequence for real part but the imaginary approximately equal to zero and can be neglected.

The real value-FFT is feed by one input real only and set the imaginary equal to zero, so half operation is used and half the FFT length. The mathematical equation of real value FFT is represented as in equation 4.3 below:

$$X[k] = \sum_{n=0}^{N-1} x[n] e^{-j\left(\frac{\pi}{N}\right)nk}, \quad k=0,1,2,\dots, N-1 \quad (4.3)$$

The input $x[n]$ is only real as in equation (4.4)

$$\text{Im}(x[n]) = 0 \quad (4.4)$$

The difference between the real and complex value FFT is the operation time divided by two, so the missing number 2 in the exponential of the equation above when compared with complex FFT equation [109].

CHAPTER FOUR *IMPLEMETATION OF THE OFDM TRANSCEIVER MODEL*

The output FFT is a complex conjugate of $X[k]$ as in equation (4.5).

$$X[N - k] = X^*[k] \quad \text{for } K=1, \dots, N/2-1 \quad (4.5)$$

Therefore, instead of computing the N -point FFT which required $(N/2) \cdot \log_2(N)$ complex multiplications and $N \cdot \log_2(N)$ complex additions, in real value FFT, we only have to compute $(N/2)$ -point FFT and perform extra $(N/2)$ complex addition and multiplications as in equation (4.6) [111].

$$\text{Computational Complexity} = (N/2) * \log_2\left(\frac{N}{2}\right) \quad (4.6)$$

The analysis equations for the number of Complex Additions of N point IFFT is described below:

$$\text{Complex Additions} = \frac{N}{2} \log_2\left(\frac{N}{2}\right) + N =$$

$$\frac{N}{2} (\log_2 N - \log_2(2)) + (N) \log_2(2) =$$

$$\left(\frac{N}{2}\right) (\log_2 N) + \left(-\left(\frac{N}{2}\right) + N\right) =$$

$$\frac{N}{2} \log_2(N) + \left(\frac{N}{2}\right) \log_2 2 = \left(\frac{N}{2}\right) (\log_2(N) + \log_2 2)$$

$$= (N/2)(\log_2(2N))$$

The number of Complex Multiplication as in equation below:

$$\text{Complex Multiplication} = \frac{N}{4} \log_2\left(\frac{N}{2}\right) + \frac{N}{2}$$

$$= \frac{N}{4} (\log_2(N) - \log_2(2)) + \frac{N}{2} \log_2(2)$$

$$\begin{aligned}
 & \frac{N}{4} \log_2(N) + \left(\frac{-N}{4} + \frac{N}{2} \right) \log_2(2) \\
 &= \frac{N}{4} \log_2(N) + \left(\frac{-N+2N}{4} \right) \cdot \log_2(2) \\
 &= \frac{N}{4} \log_2(N) + \frac{N}{4} \log_2(2) \\
 &= (N/4) \log_2(2N)
 \end{aligned}$$

In this method, the parallel data input for the imaginary part is organized into different ent group which is set symmetrically. Firstly, the first set is starting from (0 to ((N/2)-1) and feeding directly to IFFT with no change. The second group of data input ordered in reverse the first group direction which is start from ((N/2)-1 to 1).

$$\begin{cases} X \left(1 \text{ to } \left(\frac{N}{2} \right) - 1 \right) \\ X \left(\left(\frac{N}{2} \right) + 1 \text{ to } N \right) \end{cases} = \begin{matrix} X(K) \\ X^*(K) \end{matrix} \quad (4.7)$$

The equation 4.7 above discusses the parallel imaginary input to IFFT which is divided into two group. The first one in the group X(1) equals the last in the second part of the group X(N), and the last one X(N/2-1) in the first group equals X(N/2+1) for the second set. Furthermore, the two-input position is real X (0), X (N/2) which set the imaginary part input equal to zero for these two points.

The output OFDM symbol from IFFT is real with imaginary part small and can be ignored. The advantage of this method is not used IQ modulator to mix real and imaginary part of the signal and transmitted over the channel [39].

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The benefits of real value are reduced the processing operation for OFDM system. The data received is fed directly to FFT, but the output result from FFT is symmetric data. The simple block diagram represents the process above as in **Figure 4-2**.

The using length of IFFT/FFT 256 the input $X(1)$ and $X(128)$ Real only so the imaginary part zero. The data input from $X(2)$ to $X(127)$ stayed the same and connected after $X(128)$ to start from $X(127)$ to $X(2)$. The output result is real symmetric conjugate only, and the imaginary part is small and approximately zero so it can be neglected. The output from the IFFT is two parts but the same sequence.

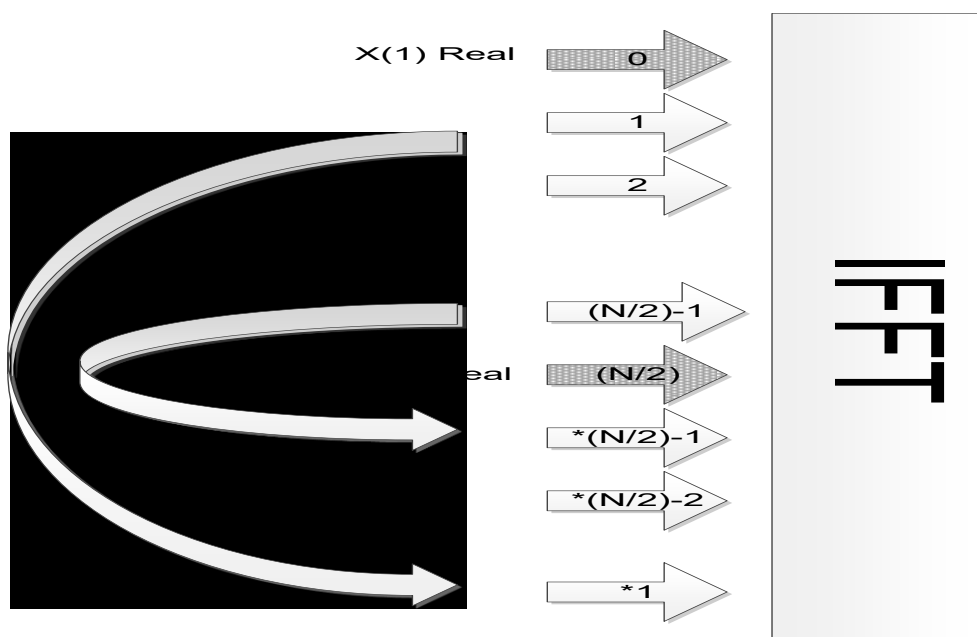


Figure 4-2 Real Value IFFT data input for imaginary part

The real part input to the IFFT is a double up as in **Figure 4-3** the input is real value subcarriers with double-up the input and not conjugated.

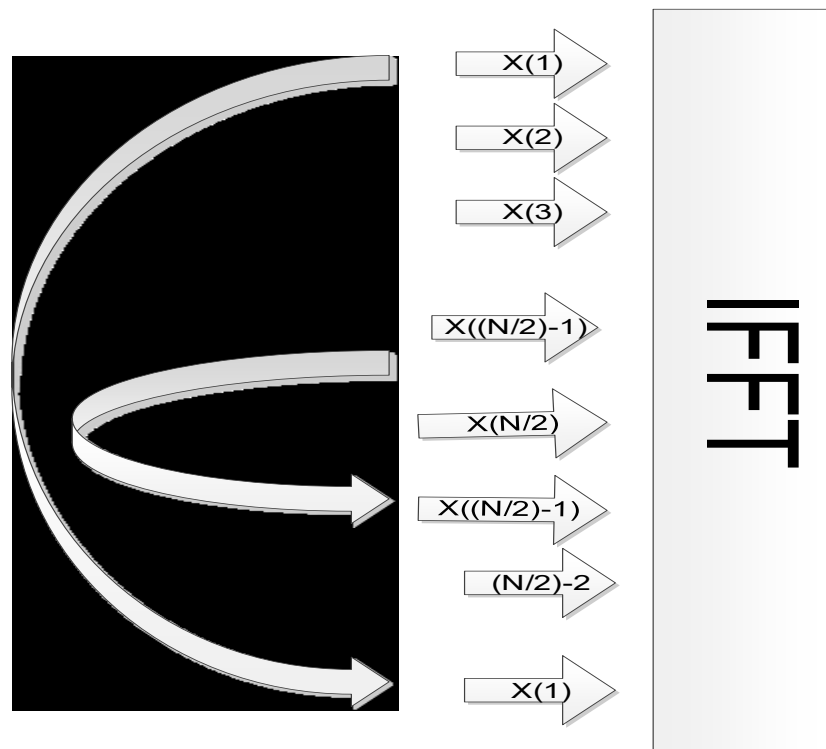


Figure 4-3 Real value IFFT data input for real part

4.3 System setting parameters

This section has discussed the setting of the OFDM model implementation by using Simulink Xilinx System Generator. The parameters setting includes the bit rate, frequency, modulation subcarriers type, and subcarriers number used to feed IFFT. The two OFDM model experiments are implemented Complex value OFDM, and Real value OFDM by depends on the output from IFFT. The various parameters are applied to each design model above (real and complex). The researched parameters such as Cyclic Prefix length, IFFT/FFT length, Number of bit precision, Symbol rate, and the modulation types. All these parameters will be discussed in the following section in this chapter.

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The settings parameters of the complex value OFDM design model are described below:

Symbol rate = 100×10^6 symbol/s

Subcarrier frequency = 100 Mhz.

QPSK carrier carry = 2 bit/subcarrier

16QAM carry = 4 bit/subcarrier

Bit rate QPSK = $2 \times 100 \text{ Msymbol/s} = 200 \text{ Mb/s}$.

Bit rate 16QAM = $4 \times 100 \text{ Msymbol/s} = 400 \text{ Mb/s}$.

Bandwidth = $2 \times \text{Carrier frequency} = 2 \times 100 \text{ Mhz} = 200 \text{ Mhz}$

OFDM Symbol Duration = Cyclic Prefix + Symbol duration.

Subcarriers Number = 256.

$$\text{SubCarrier spacing} = \frac{\text{Subcarrier frequency}}{\text{Number of Subcarriers}} = \frac{100 * 10^6 \text{ Hz}}{256} = 390625 \text{ Hz}$$

OFDM Symbol duration = Useful symbol time + Cyclic Prefix Time

$$\text{Useful symbols time } T_{\text{IFFT}} = \frac{1}{\text{Subcarrier spacing}}$$

$$T_{\text{IFFT}} = \frac{256}{100 * 10^6} = 2.56 \mu\text{s}$$

$$\text{One subcarrier time} = T_{\text{IFFT}} / N_{\text{IFFT}}$$

In our experiment calculation uses IFFT with length = 256.

$$\text{One subcarrier time} = \frac{2.56 \mu\text{s}}{256} = 10 \text{ ns}$$

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Using 25 Cyclic Prefix subcarriers :

$$\text{Total subcarier duration} = \text{No. of CP} * \text{duration of one subcarrier}$$

$$= 10 * 10^{-9} * 25 = 0.25\mu s$$

$$\text{OFDM Symbol duration} = 2.56\mu s + 0.25\mu s = 2.81\mu s$$

$$\text{Data Rate} = \frac{\text{Number of encoded bits per OFDMsymbol}}{\text{OFDM Symbol Duration}} =$$

$$\frac{\text{No. of active Sub} * \text{No. of Bit} * \text{coding rate}}{\text{OFDM Symbol duration}}$$

No. of active subcarriers = total number of subcarriers-CP=256-25=231.

The bit rate of the complex value OFDM symbol using different modulation formate as in equation below:

$$\text{for 16QAM} = \frac{231 * 4 * 0.5}{2.81\mu s} = 164.4128 \frac{\text{Mbit}}{s}$$

$$\text{for QPSK} = \frac{231 * 2 * 0.5}{2.81\mu s} = 82.2064 \text{ Mbit/s}$$

The result above shows that the bit rate of the OFDM symbol using 16QAM is significantly higher than the QPSK by a factor of 2.

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The parameters and equations which describe the real value OFDM model are shown below:

Symbol rate= 100 Msymbol/s

Subcarrier frequency =100 Mhz.

QPSK carrier carry= 2 bit/subcarrier

16QAM carry= 4 bit/subcarrier

Bit rate QPSK = 2*100Msymbol/s= 200 Mb/s.

Bit rate 16QAM =4*100Msymbol/s= 400 Mb/s.

Bandwidth = 2*Carrier frequency =2*100Mhz=200Mhz

OFDM Symbol Duration= Cyclic Prefix + Symbol duration.

Subcarriers Number=**128**.

$$\text{SubCarrier spacing} = \frac{\text{Subcarrier frequency}}{\text{Number of Subcarriers}} = \frac{100 * 10^6 \text{Hz}}{128} = 781250 \text{Hz}$$

OFDM Symbol duration = Useful symbol time + Cyclic Prefix Time

$$\text{Useful symbols time } T_{\text{IFFT}} = \frac{1}{\text{Subcarrier spacing}}$$

$$T_{\text{IFFT}} = \frac{128}{100 * 10^6} = 1.28 \mu\text{s}$$

$$\text{One subcarrier time} = T_{\text{IFFT}} / N_{\text{IFFT}}$$

In our experiment uses IFFT with length =256.

$$\text{One subcarrier time} = \frac{1.28 \mu\text{s}}{256} = 5 \text{ns}$$

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Using 25 Cyclic Prefix subcarriers:

$$\text{Total subcarier duration} = \text{No. of CP} * \text{duration of one subcarrier}$$

$$= 5 * 10^{-9} * 25 = 0.125\mu s$$

$$\text{OFDM Symbol duration} = 1.28\mu s + 0.125\mu s = 1.405\mu s$$

$$\text{Data Rate} = \frac{\text{Number of encoded bits per OFDMsymbol}}{\text{OFDM Symbol Duration}}$$

$$\frac{\text{No. of active Sub} * \text{No. of Bit} * \text{coding rate}}{\text{OFDM Symbol duration}}$$

$$\text{No. of active subcarriers} = \text{total number of subcarriers} - \text{CP} = 128 - 25 = 103.$$

$$\text{for 16QAM} = \frac{103 * 4 * 0.5}{1.405\mu s} = 146.62 \frac{\text{Mbit}}{s}$$

$$\text{for QPSK} = \frac{103 * 2 * 0.5}{1.405\mu s} = 73.31 \text{ Mbit/s}$$

The conclusion from the equations analysed above the spacing of the subcarriers is increased to double when using Real Value OFDM. In real value OFDM the number of subcarriers is reduced to half when compared with complex value OFDM and a significant decrease of real value OFDM symbol rate. The reduction in symbol rate between real and complex value OFDM symbol when using 16QAM is 18.2%. The OFDM symbol rate reduced to 9% when using QPSK subcarriers modulation type for the example above.

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The block diagram in figure **Figure 4-4** shows the process of the design model of each block in this model is translated to Simulink block using Simulink Xilinx System Generator. The general description of the OFDM experiment is described as follows:

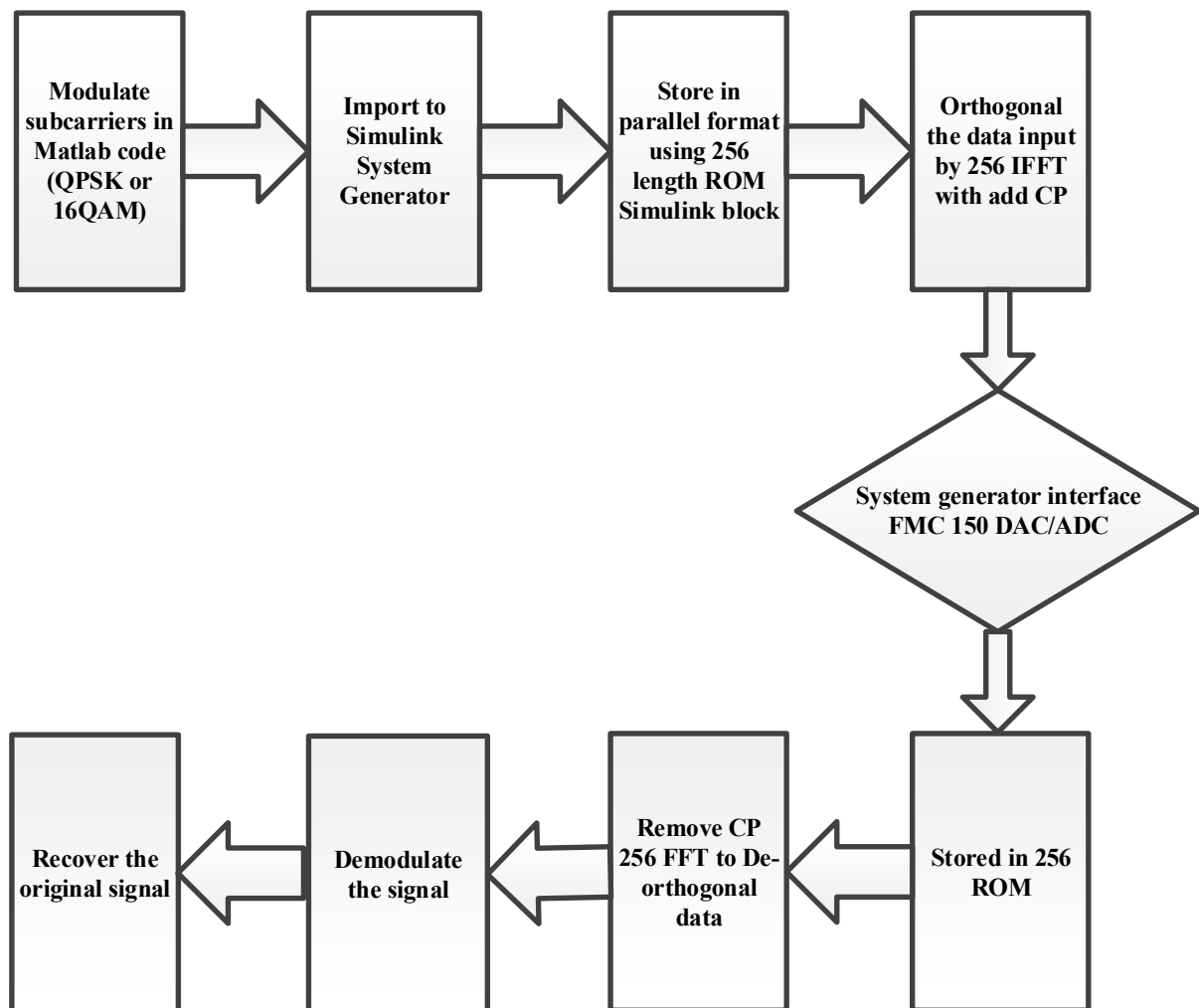


Figure 4-4 OFDM block diagram.

In this experiment uses 256 points IFFT length which is organised subcarriers by 256 parallel inputs to IFFT including spaces of CP.

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The design starts by counting parallel subcarriers number by reading ROM address which is loaded a frame of QPSK or 16 QAM encoded subcarriers signal from Matlab code. The encoded subcarriers are feed to the Simulink model by loading the subcarriers into a single port ROM. This data is read in a parallel format from the ROM Xilinx Simulink block with a length equal to the length of IFFT. The output data from the IFFT is an OFDM Symbol in parallel format with CP. This Symbol is converted to serial and moving through the Simulink DAC/ADC block Gateway. The block is used Simulink System Generator tool to simulate the DAC/ADC using the I/O gateway with an option of DAC/ADC. The signal on the receiver side stored in ROM then feeds to the FFT with all the control signals connected directly from IFFT to FFT.

The Matlab library code uses to generate QPSK subcarriers for the modulator for a specific setting. The Matlab code uses system object as shown below to generate a modulated signal

comm.QPSKModulator

In the receiver side used a demodulation QPSK system object code as

comm.QPSKDemodulator

The modulator of 16QAM modulation using system object code on the transmitter side as

comm.RectangularQAMModulator

On the receiver side using a system object code as in the code below

comm.RectangularQAMDemodulator

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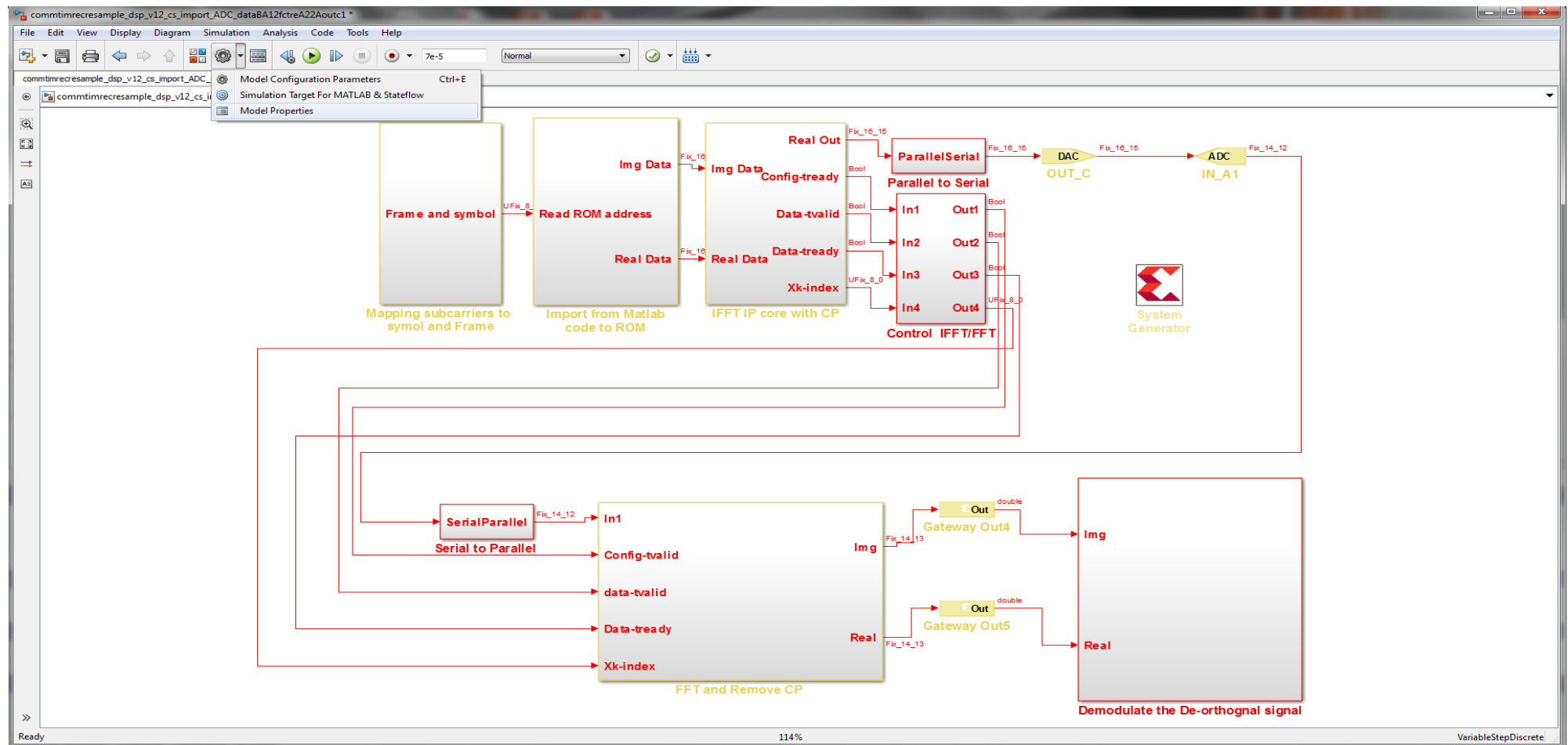


Figure 4-5 OFDM Matlab Simulink Blocks

To import the Matlab code to the Simulink blocks by using Matlab Simulink environment main window as follows:

*Tool>Model Explorer> Callbacks>PreloadFcn**

In PreloadFcn select a name of Matlab code function which contains a code for generating QPSK or 16QAM encoded subcarriers.

Figure 4-5 shows the Simulink OFDM model block with the procedure describes how to import subcarriers generated in Matlab code to Simulink. The figure above contains the main Simulink block of generating OFDM symbols in the transmitter and demodulator in the receiver with an additional block to control the signal between IFFT/FFT. The parallel OFDM symbols are converted to serial and transmitted through the DAC/ADC converter. The demodulated signal is sent back to the Matlab code for demodulation and recovers the original signal.

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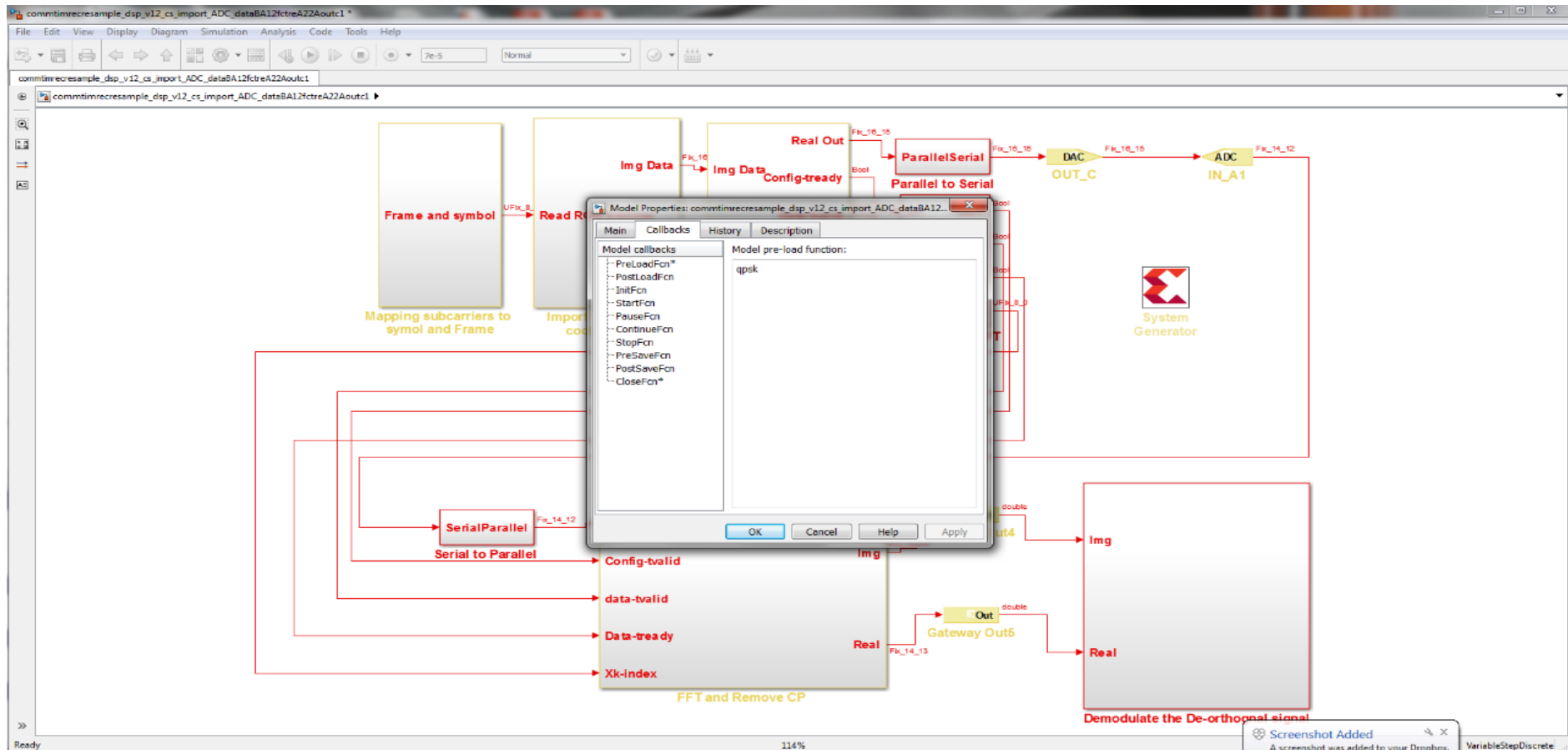


Figure 4-6 preload function to import encoded subcarriers

Figure 4-6 shows the procedure to import subcarriers from Matlab code to Simulink System Generator by using the *PreLoad* function. This option is allowing Simulink to call the function when starting a Simulink model. Therefore, all subcarriers (QPSK, 16QAM) are available in the workspace of Matlab and ready to be used by the Simulink block.

The encoded subcarriers (QPSK, 16QAM) are imported from the Matlab code which is stored in the Xilinx Simulink Block ROM cells of a size equal to the length of the IFFT.

To read the address of the ROM described above, a combination of Xilinx System Generator blocks are used. These blocks include the following: a counter, an arithmetic relationship operator, and a Bus Multiplexer as shown in **Figure 4-7**.

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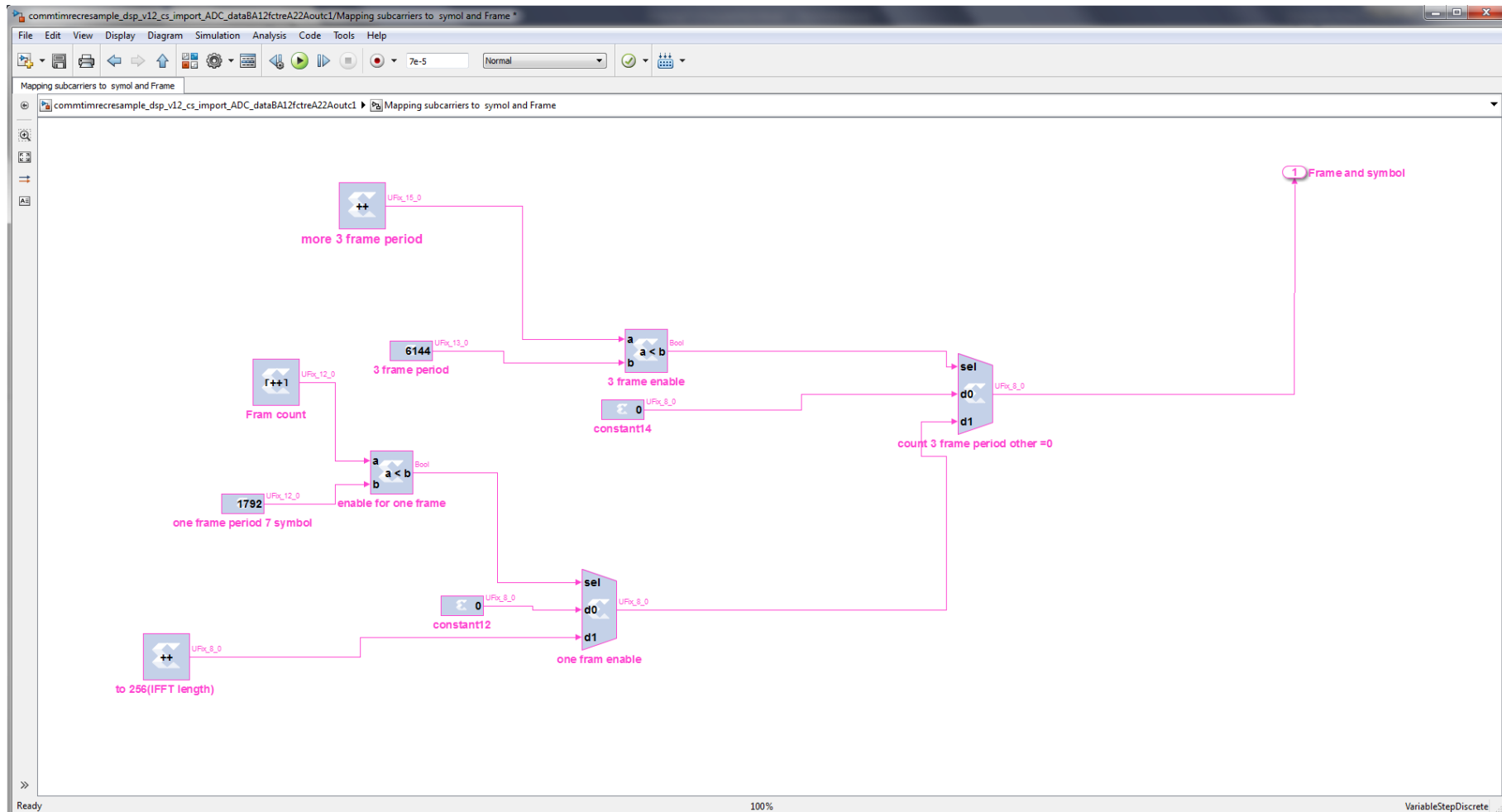


Figure 4-7 Parallel data arrangement to read from ROM

The output from the blocks above is used to read the ROM cell address which stores the subcarriers and is equal to the length of the IFFT. However, the parallel frame length input to IFFT is excluded the length of CP subcarriers. For example, when using 25 length CP, the subcarriers carry data equal to

$$\text{Active Subcarriers} = N_{IFFT} - CP \quad (4.8)$$

256-25=231 subcarriers carry data

The other subcarriers (CP spaces) are set to zero, so the total number of subcarriers is equal to the length of the IFFT. The setting of the Xilinx blocks is shown in **Figure 4-8**.

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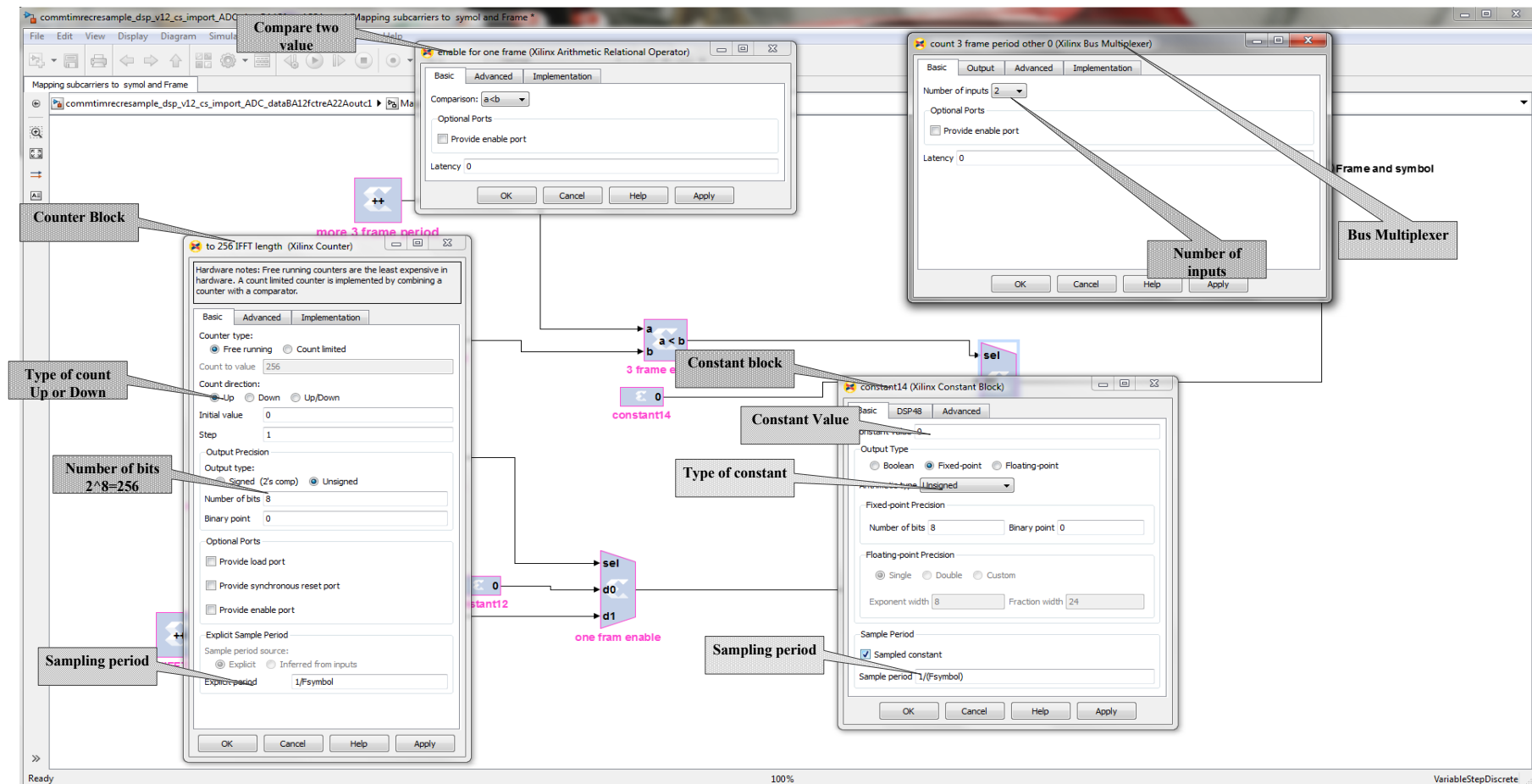


Figure 4-8 Description setting of Simulink Blocks

The counter starts to count the number of subcarriers which is equal to the IFFT length, with word length width equal to 8 bits. The subcarriers use unsigned fixed-point word length bit width type and selected 8 bits word length width because of $\text{IFFT} = 256$ points, then $\log_2(256) = 8$.

The IFFT type is used Pipeline streaming-IO with clock frequency 100Mhz. However, The IFFT input length is varied and depends on the subcarriers number used that is saved in ROM before IFFT. The connection point of the IFFT Simulink to The Xilinx Simulink IFFT IP core setting by set a constant input to IFFT at point (s_axis_config_media_fwd_inv) equal to zero. The input subcarriers feed to the IFFT uses the point terminal (xn_img, xn_re) which is received the imaginary and real part of the subcarriers respectively. The length of the Cyclic Prefix is added to the OFDM symbol through the IFFT port which is included an option for adding CP with IFFT Xilinx block. The CP length is simulated by using constant type Xilinx Simulink block with bit word length unsigned fixed equal to $\log_2(\text{NFFT})$. The encoded signal is processed inside the IFFT with delay, so a new parallel data frame is waiting until process finishing to generate an OFDM symbol then loaded a new frame of data. Therefore, when IFFT process finish a signal output (s_axis_tready) is active high which sending a feedback signal to IFFT and going to Tvalid which allowed loading a new frame of data again.

del as in **Figure 4-9**.

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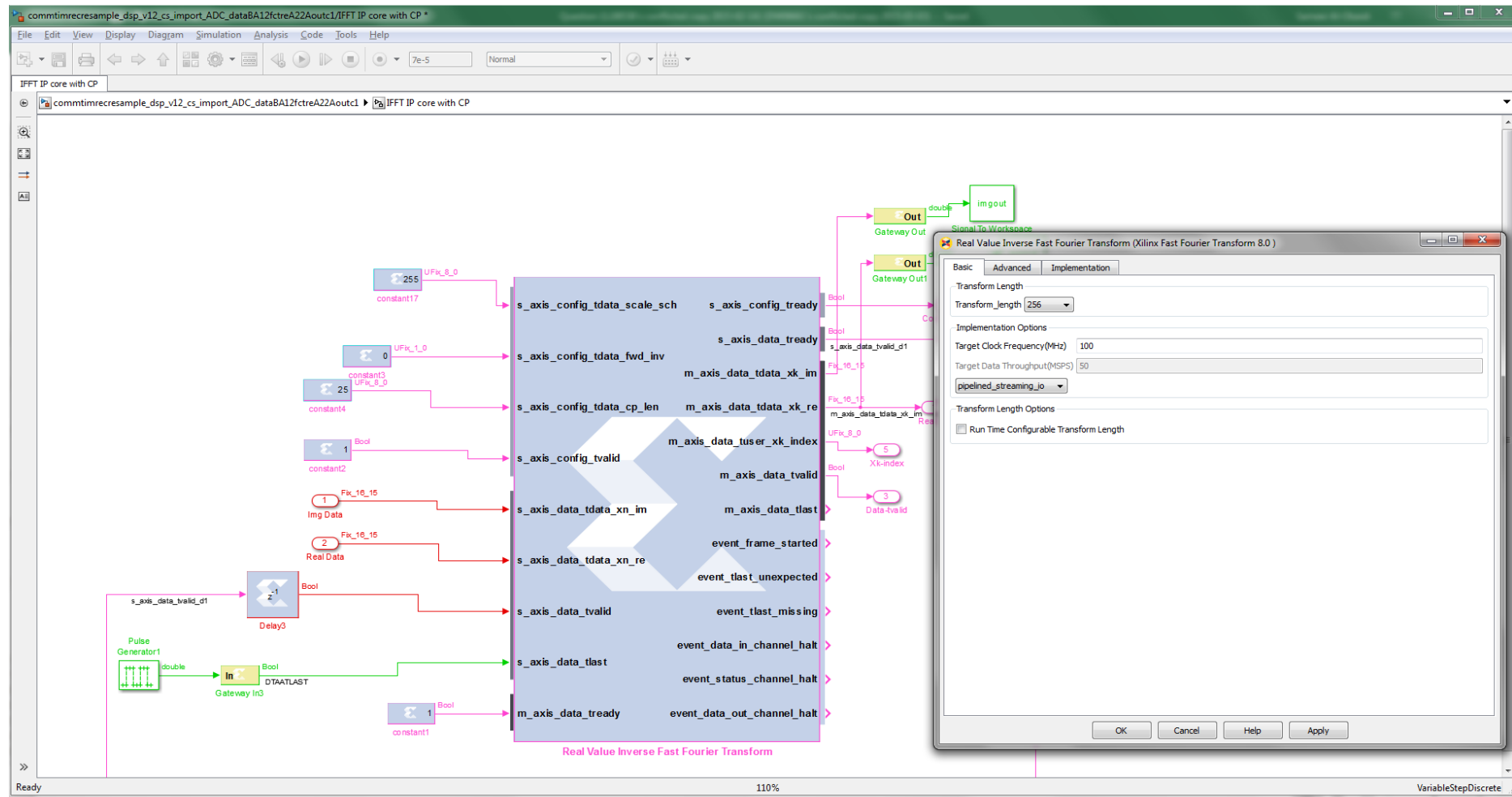


Figure 4-9 IFFT configuration of the design

The type of signal output from IFFT is an OFDM symbol in parallel format with word length equal to the IFFT input because of uses a scale type. The OFDM symbol is converted to serial and transmitted as an analogue by DAC the received OFDM symbol is converted to digital by ADC.

The received OFDM symbol signal is converted from serial to parallel format and remove Cyclic Prefix to enter FFT. This part of the receiver is used to de-orthogonalise the OFDM symbol. The signal is exported to Matlab code to demodulate and recover the original data signal.

The following section will be describing the simulation experiments implemented of the OFDM model above and discover the effect IFFT/FFT of an FPGA power consumption on. The various parameters applied to the model above then generate power report for IFFT/FFT with each change in the parameter. The discussion has discovered the parameters which affected on FPGA power consumption of the IFFT/FFT IP core used in OFDM model. The following section compares the power consumption of IFFT for various parameters results between two models (complex and real value OFDM models).

4.4 Real and Complex IFFT for OFDM

This section is comparing the FPGA power consumption between two OFDM models used widely in communication applications. The measurement of power consumption is focused on one part of the design IFFT/FFT which is affected by the real and complex value IFFT inside the OFDM design model. The complex value OFDM is used conventional OFDM in the design by using the normal input to IFFT and generate a complex value OFDM symbol. The real value uses the proposed model in the design to generate the real value output OFDM symbol from IFFT after feeding the IFFT with a special arrangement of input subcarriers data described in this chapter. However, the Fast-OFDM in chapter two is used as the background for this section. This technique is lower complexity than conventional OFDM. This section discovered the effect the OFDM symbol output real and complex on IFFT/FFT power consumption by comparing the FPGA power consumption of two models Complex and Real value OFDM. The output types depended on the input feed to the IFFT which symmetric or normal input. The input subcarriers used in this section to generate the real OFDM symbol are symmetric for the real part, and symmetric conjugated for the imaginary part with two locations set to zero. The Real OFDM is preferred in optical communication applications because this type uses only the real part of the signal in the transmission.

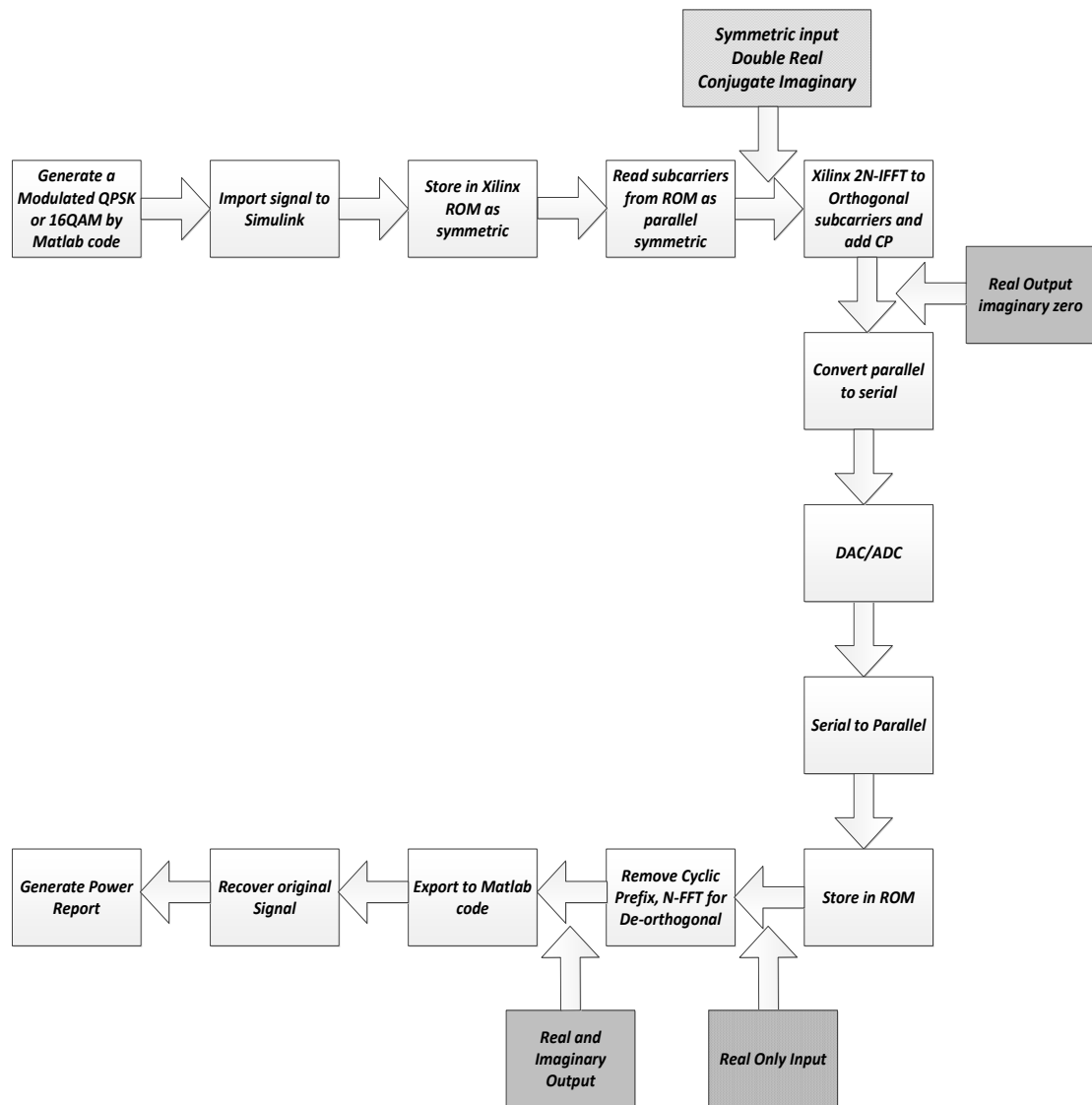


Figure 4-10 Block diagram for the Real value of OFDM

The Figure 4-10 is described the flowchart uses to generate the real value OFDM symbol. The red boxes in the block diagram on the top have described the arrangement of subcarriers before IFFT. The subcarriers frame input feed to the IFFT uses the real part by symmetric double up, but the imaginary part is conjugated and the two locations input $x(0)=0$ and $x(N/2)=0$. The number of subcarriers is equal to the double length of IFFT used. The signal generated is real value OFDM symbol with the imaginary part is significantly small and can be neglected.

The signal transmitted over D/A, A/D store in ROM on the receiver side. The OFDM symbol uses an N length FFT for de-orthogonalise the OFDM symbol which is represented by red block boxes in the bottom of the flowchart. The output frame is two parts of the subcarriers and sends to Matlab code to recover the original signal.

The power report is generated by the Xilinx System Generator for all the models with a focus on the IFFT/FFT. The power measurement of this part is sent to Excel to draw the graphs below for the experiment by comparing the power between real and complex value OFDM.

The first experiment uses 16QAM subcarriers modulation format to feed IFFT. The different number of bit precision uses from (10 to 32) bit to this experiment. The bit rate for both experiment real and complex value OFDM uses 400Mb/s. The result of the FPGA power consumption report compared between complex and real value IFFT for the OFDM model is shown in

Figure **4-11.**

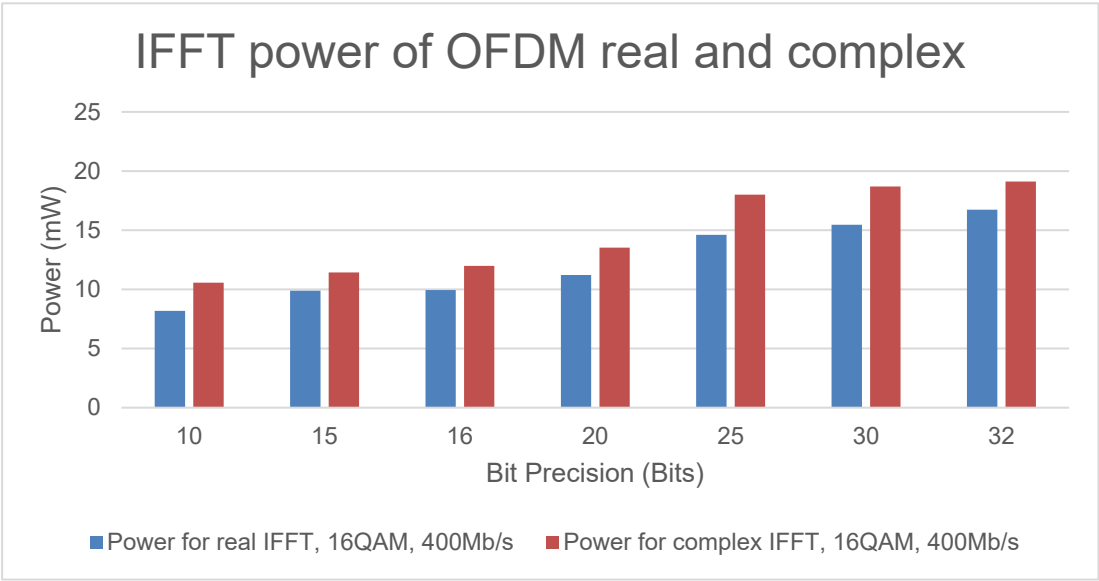


Figure 4-11 OFDM with Real and Complex IFFT using 16QAM

The result above shows the power measurement of real value is lower than the complex IFFT when using 16QAM subcarriers input to IFFT with the same bit rate of 400Mb/s. The FPGA power difference is reduced by 22.52% between the real and complex value IFFT for the first experiment of OFDM when using 10 bits in bit calculation precisions and 16QAM subcarriers modulation. The power measurement result compares the real and complex IFFT is reduced when increasing the number of bit precisions to reach 12.45% when using 32-bit precision calculations. However, in all the experiments above the power consumption of IFFT for Real value is lower than the Complex value by an average of 17%. This reduction is due to reduce the complexity of DSP inside IFFT by reducing the number of multiplications and additions to generate an orthogonal OFDM symbol.

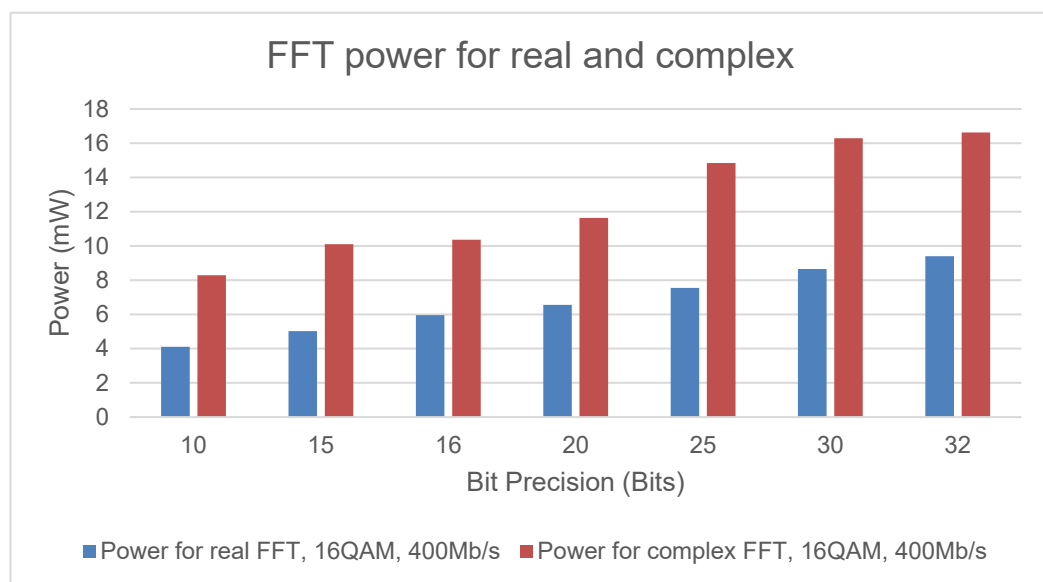


Figure 4-12 FPGA power of real and complex FFT with 16QAM

On the receiver side, the FPGA power consumption of the FFT for 16QAM and bit rate 400Mb/s to generate the OFDM symbol is described in **Figure 4-12** above.

The input feed the FFT is only a real OFDM symbol and set the imaginary equal to zero. The reduction power between real and complex value FFT for the first experiment is 52.42% when using 10 bit in precision calculations for both experiments. The reduction in power is 43.48% when using 32-bit precision calculations. The average power reduction for all experiment of FFT 46.6%. This reduction is due to the calculation occurs only for OFDM real part of the input to FFT which reducing the DSP processing such as multiplication and addition inside FFT.

The comparing power measurement result of IFFT with another type of subcarriers feed to it such as QPSK instead of 16QAM is used to generate the OFDM symbol. The experiment is implemented when change subcarriers modulation using QPSK with bit rate 200Mb/s. The sampling frequency is used 100Mhz is same for both experiments. The FPGA power measurement result is compared Complex and Real value IFFT which implemented on OFDM subcarriers modulated by QPSK is in **Figure 4-13**.

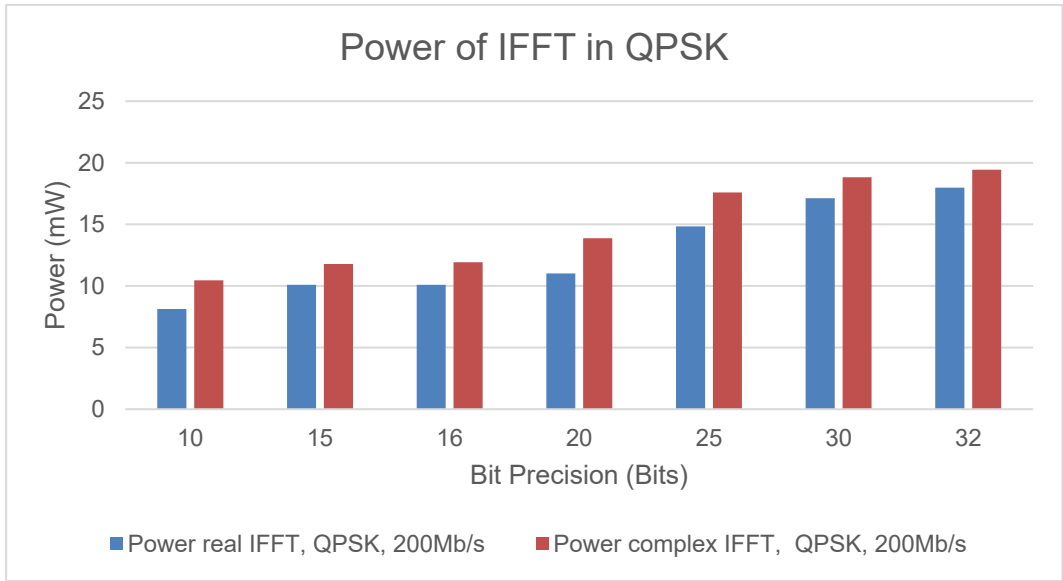


Figure 4-13 OFDM with QPSK Real and Complex

The result shows the FPGA power is reduced when using QPSK subcarriers of real value IFFT instead of complex value. The difference in power reduction between real and complex IFFT for 10-bit precisions calculation is 22.18%. The average difference between real and complex for all experiment using QPSK with 200MB/s is 15%. The reduction is due to reducing the complexity and DSP processing of the IFFT to produce only the real part of the OFDM symbol.

The power consumption result which compares between QPSK and 16QAM subcarriers to generate OFDM symbol in real and complex for IFFT. The FPGA power result shows the same percentage difference between real and complex OFDM symbol with 10-bit precision which is approximately 22%. The average power consumption of IFFT with 16QAM is 17% and for QPSK is 15%. The small difference in average power consumption difference 2% lower when using QPSK subcarriers is due to lower bit carry per subcarrier in QPSK. The FPGA power consumption of the FFT in the receiver side of the OFDM transceiver for the same setting above by using QPSK subcarriers as in **Figure 4-14**

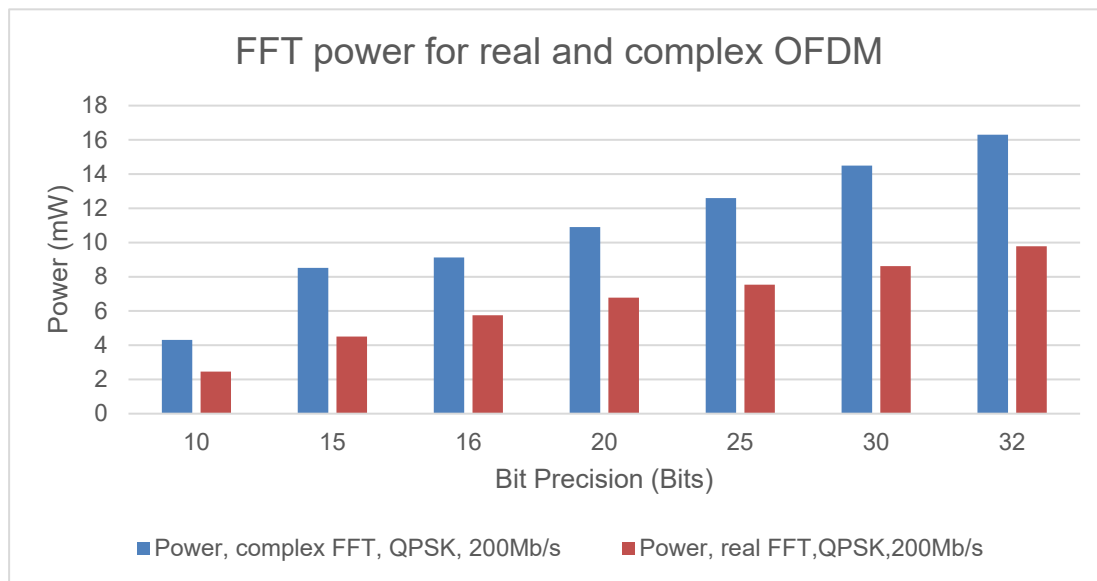


Figure 4-14 FPGA power for FFT of OFDM symbol with QPSK

The result shows the power of the real FFT is lower than the Complex FFT for half power because the input uses only real part and set the imaginary part to zero. The percentage difference between FFT to de-orthogonal OFDM real and complex symbol is 43% when using 10 bit and the difference decrease to 39% when using 32-bit precision calculation.

The average FPGA power reduction for FFT when using real value OFDM symbol generated by QPSK is 40% for experiment implemented. The difference between real and complex value is due to processing the real part of the OFDM symbols. Therefore, the processing for DSP including additions and multiplications is reduced.

The FPGA power consumption reduction of FFT for the two experiment. The reduction result is 52% when using 10 bits and QPSK and 43% for OFDM symbol with QPSK. The average reduction in FPGA power of FFT for 16QAM is 46% and for QPSK is 40%.

The power consumption reduction is 6% in FPGA between real and complex FFT. This reduction is due to processing only real part of the signal, and the number of bits carry by the OFDM symbol which affected on the processing inside FFT.

4.5 Bit Precision

The main central processing part of OFDM techniques is the IFFT/ FFT, and it is an essential part used in the transmitter, receiver respectively. Therefore, the main idea behind using IFFT/FFT to orthogonal /de-orthogonal the encoded subcarriers [25][46]. In this section has discovered the effect of phase factor bit precisions on FPGA power consumption used in the calculation of IFFT/FFT. The OFDM transceiver is implemented using the Simulink Xilinx System Generator interface with Matlab 2012b. The OFDM main block diagram of the transmitter and receiver is shown the **Figure 4-15**.

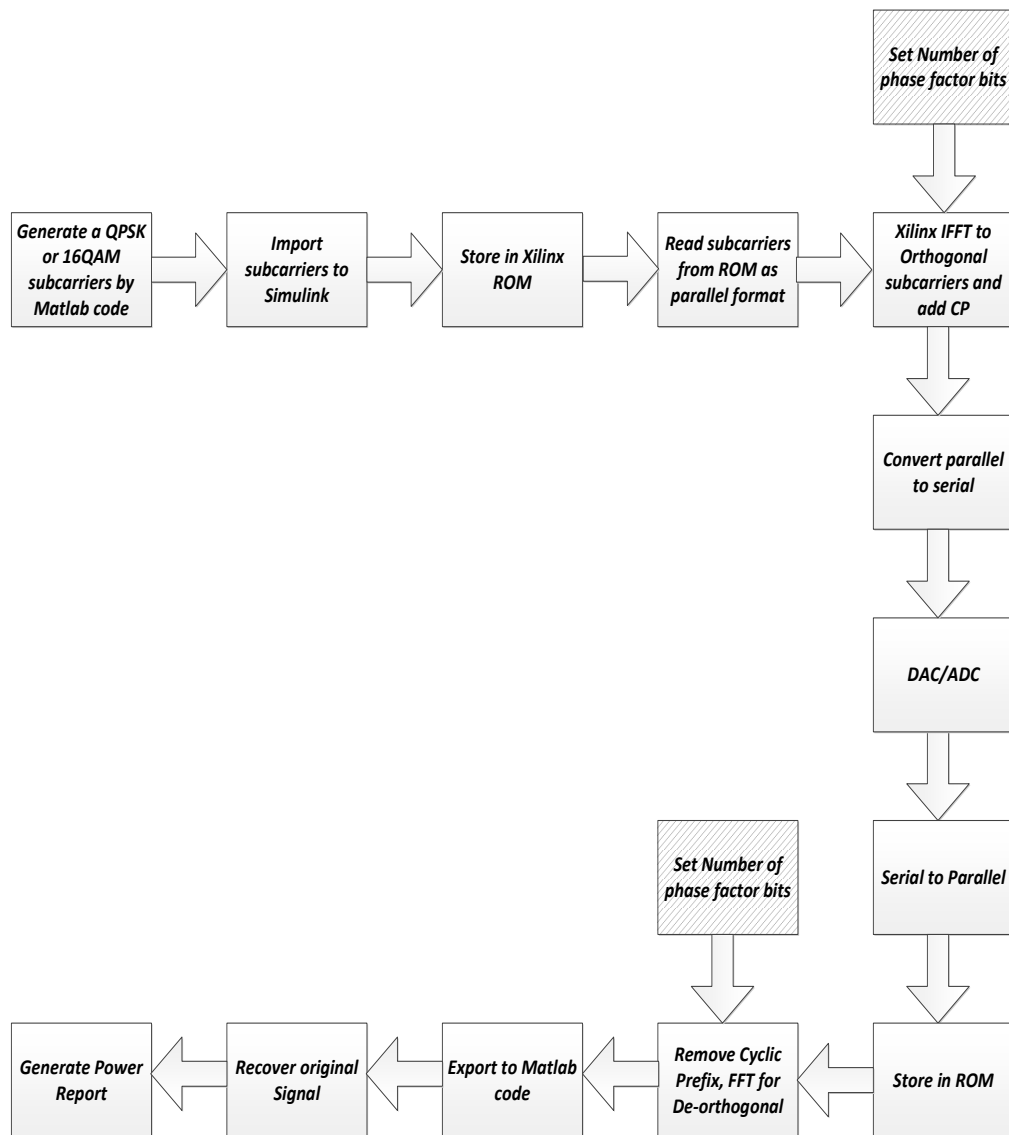


Figure 4-15 Block diagrams of the OFDM phase factor bit precision

The block diagram above describes the OFDM transceiver which includes the two essential parts for the design IFFT/FFT. The setting of phase factor bit precision has set inside IFFT on the transmitter and FFT on the receiver. The red box on the top of the IFFT in the transmitter side, and FFT in the receiver side show the location to change the bit precision. The setting of the Simulink IFFT Xilinx IP core block is shown in **Figure 4-16**.

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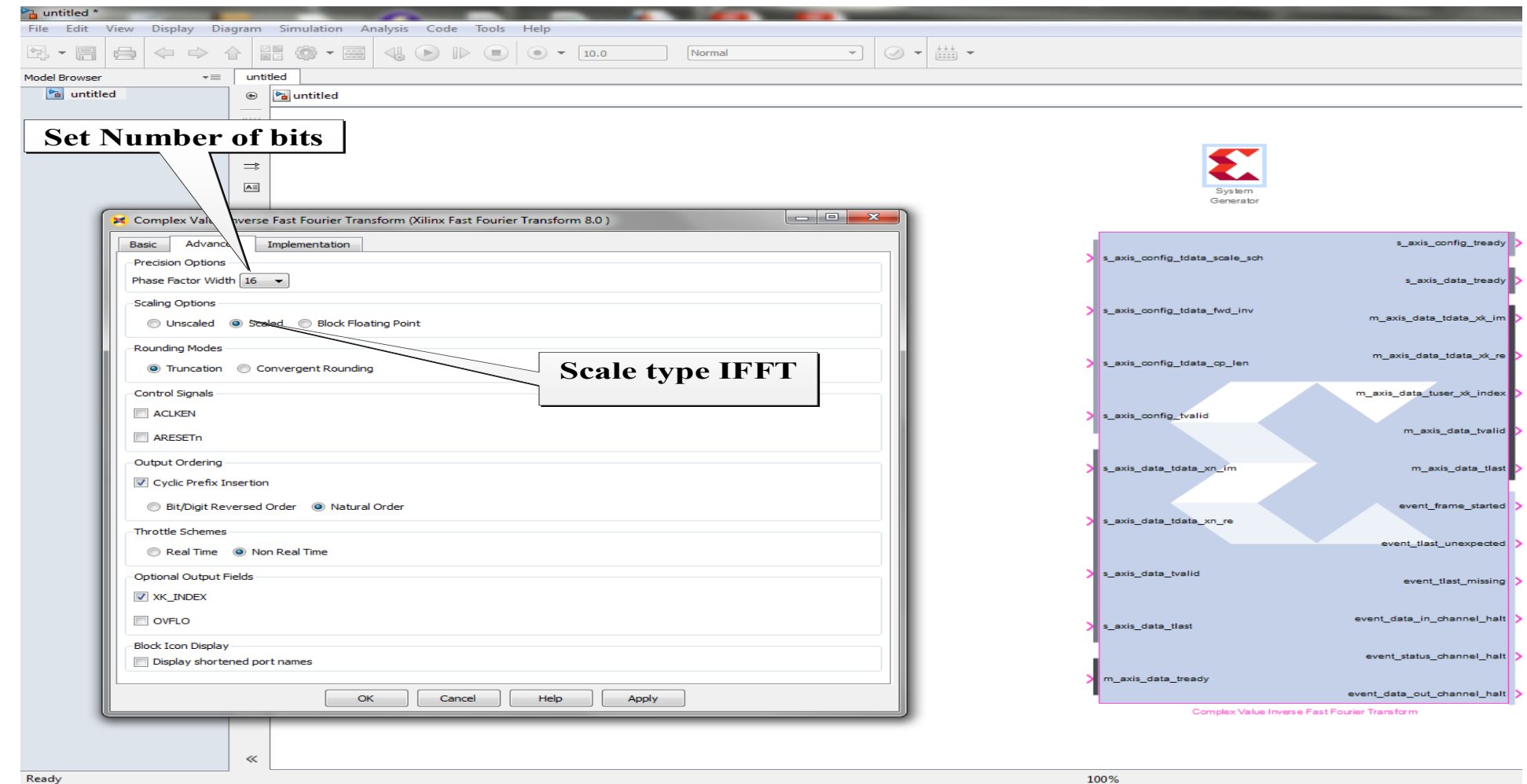


Figure 4-16 FFT Xilinx Simulink block bit width.

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The selected number of bits precision occurs inside Xilinx IP core IFFT/FFT block of the system generator and can be changed for each simulation experiment. The bit numbers has decreases or increases which is affected by phase factor precision calculation. The type of output word length width from IFFT is not affected and remain at the same input word length of the IFFT Simulink block because using Scale type IFFT. The advantage of increasing the number of phase factor bits to increase the accuracy of the IFFT/FFT calculation.

The definition of phase factor precision is a bit number used in the calculation of the exponential of the equation (4.9) [72] for complex FFT:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{\frac{-jnk2\pi}{N}} \quad k=0,1,\dots,N-1 \quad (4.9)$$

Where

N: is the transform size,

$$J = \sqrt{-1}$$

$$e^{j2\pi nk/N}: \cos(2\pi nk/N) + j \sin(2\pi nk/N)$$

$x(n)$ is the OFDM symbol generated by complex IFFT as in the equation (4.10)

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k) e^{\frac{jnk2\pi}{N}} \quad n=0,1,\dots,N-1 \quad (4.10)$$

$X(K)$: is the complex value subcarrier modulated.

For Real value OFDM, the equation is changed because used half of the input data and set the imaginary part zero for FFT, so the time is divided by 2.

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-\frac{jnk\pi}{N}} \quad k=0,1,\dots,N-1 \quad (4.11)$$

For Real value OFDM (IFFT) used in this experiment is described as in the equation 4.12

$$X[n] = \frac{1}{N} \left\{ \text{Re}(X(0)) + \sum_{k=1}^{\frac{N}{2}-1} X(k) e^{\frac{j2\pi nk}{N}} + \text{Re}\left(X\left(\frac{N}{2}\right)\right) + \sum_{k=\frac{N}{2}+1}^{N-1} X(N-k)^* e^{\frac{j2\pi nk}{N}} \right\} \quad (4.12)$$

The equations of real value had described above show the FFT is consumed lower power because using half of the input data. The subcarriers input to the IFFT is complex conjugate so the result of multiplying two complex conjugate numbers equal to real only and the complex part zero.

The encoded subcarriers used QPSK and 16QAM with 256-point IFFT/FFT length. The two models build are real and complex value OFDM which implements by Simulink Xilinx System Generator with bit precision (10 to 34) bits. Xilinx System Generator uses LogiCore IP Fast Fourier Transform Pipelined Streaming I/O which is implemented by Radix2 with Cooley-Tukey algorithm. In this experiment, uses phase factor bit precisions from (10 to 34) bits. The power report has been generated for the complete design model which shows the hierarchy power of each component such as IFFT. The power consumption result for IFFT in OFDM with Cyclic Prefix length 25 and precision 16 bit of QPSK subcarrier modulation is shown in power report **Figure 4-17**. The FPGA power consumed by IFFT is 12.72 mW shown in the power report which displays the power of each component in the design and focusing on one part of the design.

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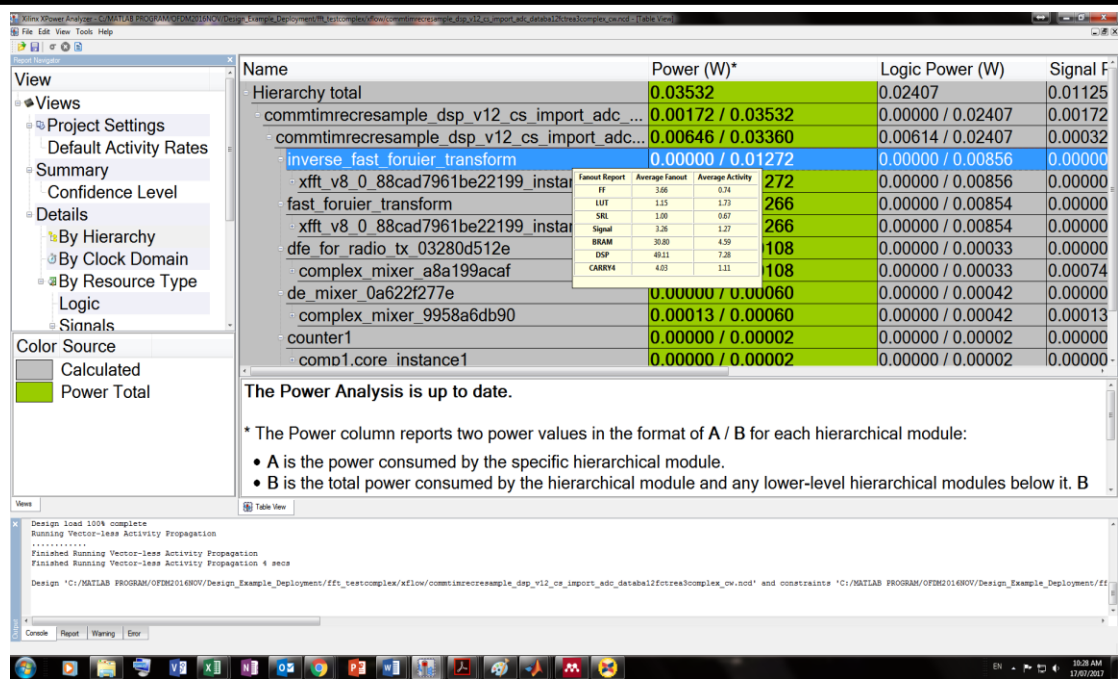


Figure 4-17 Complex OFDM model with 16bits and QPSK modulation.

The power report of the OFDM model with 32 bits precisions and using basic subcarrier modulation QPSK as in Figure 4-18. The FPGA power consumed by IFFT is increased to 21.77 mW.

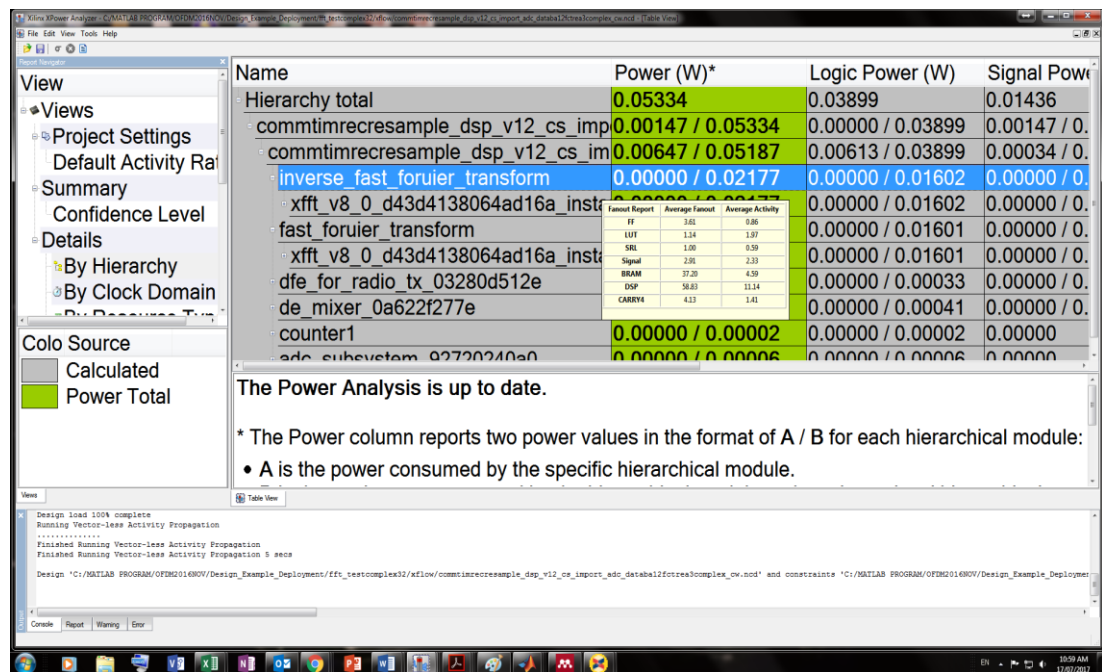


Figure 4-18 Complex OFDM model with 32bits and QPSK modulation.

The experiment is implemented by using other subcarriers modulation 16QAM instead of QPSK. The power consumption of Complex value IFFT by changing the number of bits using 16QAM modulation with 400Mb/s is described as in **Figure 4-19**. The experiments are implemented with various bit precision from (10,15,20,25,30, and 32), and the result investigates the effect of bit precision on FPGA power consumption of IFFT/FFT.

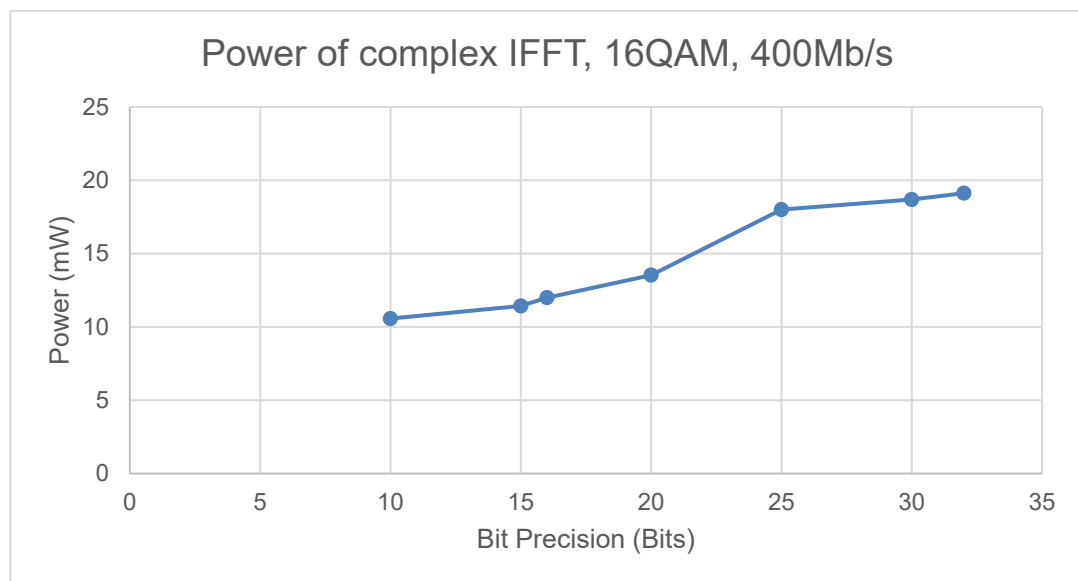


Figure 4-19 OFDM Complex IFFT Power Consumption 16QAM

The result in the figure above shows the power is increasing with increasing number of bit used in the phase factor calculation, but not linearly increase. The FPGA power consumption percentage increases by 8.14% when bits precision increase from (10 to 15) bits. The percentage is increased with increasing the number of bits, so when increasing the number of bits from 16 to 32, the percentage is increased by 59.47%. This because double up the number of bit precision calculation which led to maximise the accuracy of IFFT.

On the receiver side uses the FFT to De-orthogonal the OFDM symbol. The experiment is implemented with Complex value OFDM to investigate the bit precision calculation effect on FFT power consumption. The resulting graph is shown in **Figure 4-20** for complex value FFT.

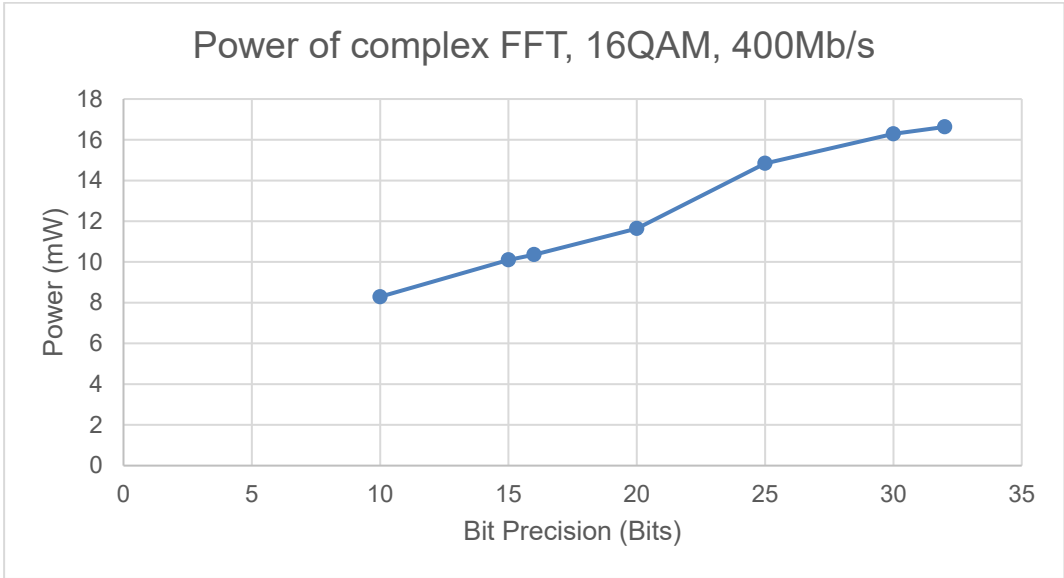


Figure 4-20 OFDM complex FFT power consumption

The power consumption result is discussed for IP core IFFT/FFT, and The result of the FFT is increased by 22% with increasing number of bit (10-15)bits with only five bits increased. The percentage of increasing power is 41% when increase bit precisions from (10-20) bit and 61% when increasing the bit precisions from (16-32) bits. This increase is due to the significant increase in the number of bits used in the calculation phase factor precisions. That means the exponential (cosine, sine) increased processing inside IFFT/FFT.

An experiment is implemented with real value OFDM as explained in the previous section with only real output from IFFT. It uses 16QAM subcarriers feed to IFFT with bit rate 400Mb/s and sampling frequency 100Mhz for the subcarriers input. The power consumption of the IFFT with various phase factor bit precision is shown in **Figure 4-21**.

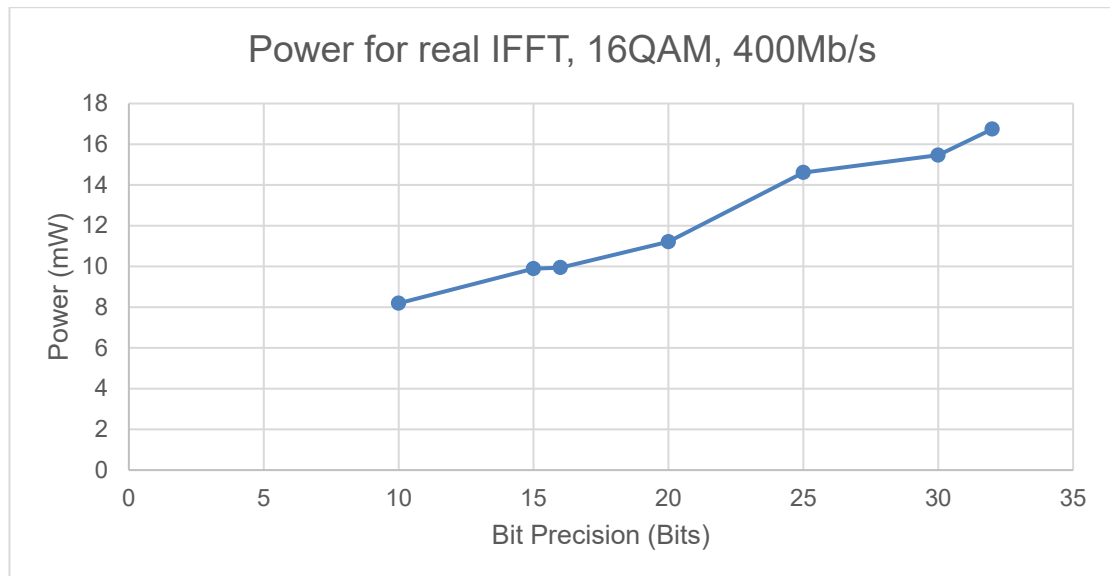


Figure 4-21 *OFDM Real IFFT power consumption*

This experiment has investigated the effect of bit precision calculation on the FPGA power consumption for real value IFFT. The result shows the power increases with bits precisions increase. The bit is increased from (10-15) bits is led to a significant increase in power by 21%. The increasing bit number from (10-20) the percentage increase 36% but this increase due to a bit from (16-32) and the percentage is increased to 41%.

To compare the result by percentage of increasing the FPGA power between real and complex value IFFT. The percentage increase with high bit precisions (16-32) bits and the result of complex value is 59.47% and in real value is reduced to 40.62% for FPGA power of IFFT.

The FPGA power consumption is increasing with bit precision for both models built real and complex value IFFT in OFDM. The increasing bit precision calculation increases the accuracy of IFFT with a significant increase in the power consumption.

The effect of phase factor bit precision on FPGA power of the real value FFT used on the receiver side of the OFDM transceiver is shown in **Figure 4-22**.

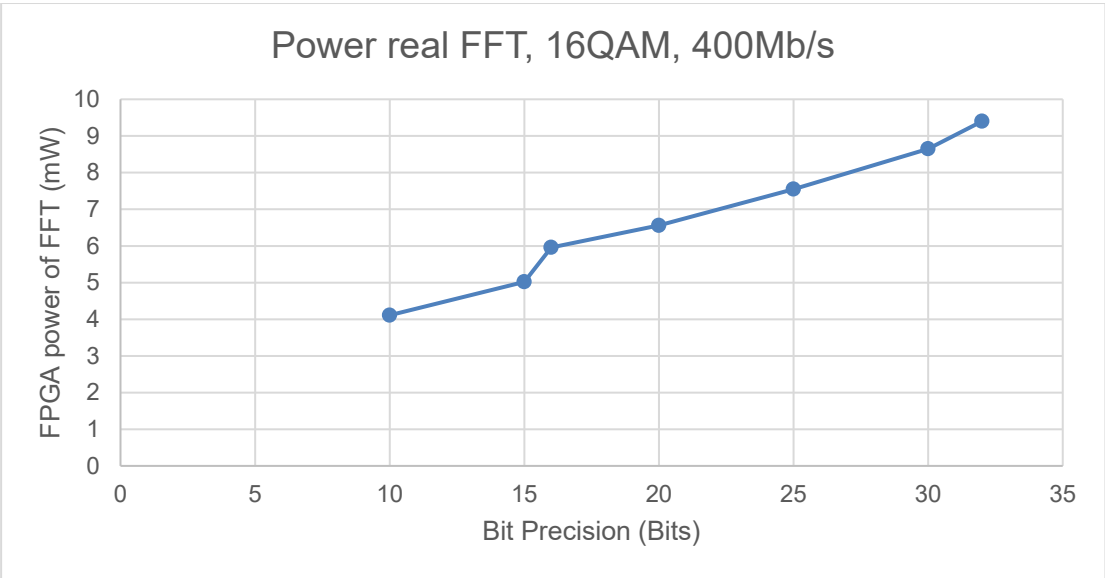


Figure 4-22 Real OFDM Power consumption of FFT

From the result, in **Figure 4-22** the FPGA power increases with a number of bit precision used in calculation phase factors for real and complex value IFFT/FFT. The power increase is described as a percentage of increasing bit from (10-12) with the 20% increase in FPGA power. In addition, increases a bit from (16-32) the percentage increases by 57%.

The power consumption result has compared between complex, and real value FFT with the percentage increase for real value and high bit precision is lower than the complex value.

A bit increase from (16-32) of the complex FFT the power is increased by 61%, and for real value FFT the power is increased by 57%. The result shows the real value FFT is efficient in power consumption than the complex value in the implementation of the OFDM.

The result compares between the transmitter and receiver of the OFDM model described as a bit error rate is shown in **Figure 4-23**.

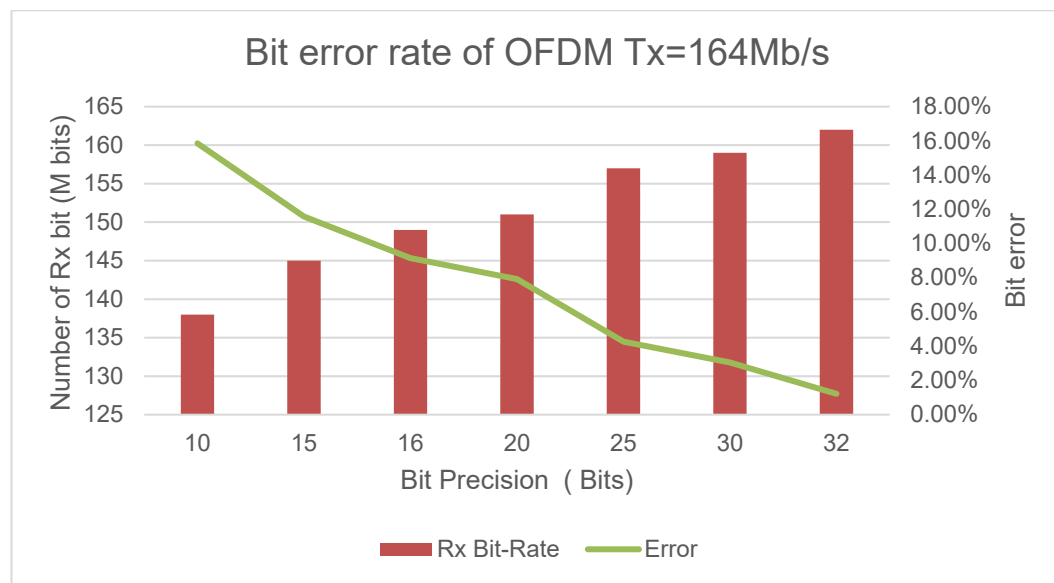


Figure 4-23 Bit error rate of the OFDM model with 16QAM

The result shows the error rate decreases with increasing the number of bits used in the calculation of the phase factor. The reducing bit precision is led to an increasing the error to 16% between transmitter and receiver. The percentage of error is reduced with increases the bit precision to 8% when using 20-bits for precision calculation. Finally, the error reduced to 2% when using full precision calculation (32 bits). The reduction in error is due to increasing the number of bits used in the bit precision calculation of the phase factor which significantly increases the power consumption for both IFFT/FFT in the OFDM model.

4.6 *Cyclic Prefix length*

Next generation high-speed multicarrier modulation uses OFDM as a base modulation technique due to the flexibility of various parameters [8]. The background for this section is provided in chapter Two which discussed the Adaptive Cyclic Prefix ACP which is effected on the transmission energy channel. The CP has increased the channel delay when increasing the CP length. In this section, discuss the CP length effect on FPGA power consumption of the IFFT (real and complex) used in OFDM model.

The OFDM modulation suffers from inter-symbol-interference (ISI) or symbols overlapping because of the short distance between OFDM symbols. The ISI occurs after processing the subcarriers to generate orthogonality by using IFFT in OFDM. Therefore, the signal distortion and noise will increase due to overlapping and the solution by adding a cyclic prefix between adjacent symbols. The procedure of adding CP by inserting a small gap which is a copy of the end of each OFDM symbol and paste at the beginning of the same symbol, but all the operation above happen after IFFT processing [11] is shown in **Figure 4-24**.

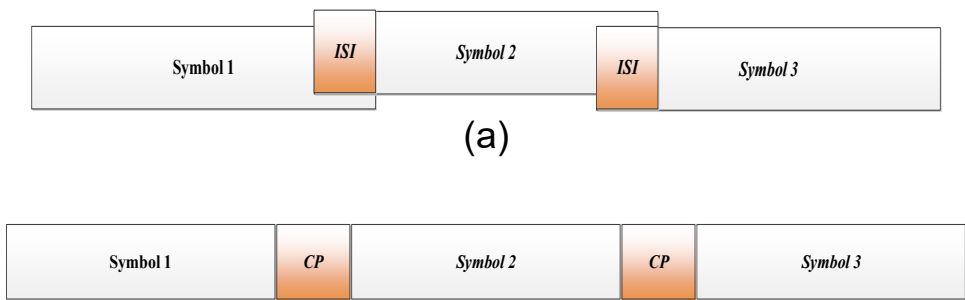


Figure 4-24 Mechanism of (a) Inter Symbol Interference ISI, and (b) Cyclic Prefix CP

A cyclic prefix mechanism can be implemented by inserting a gap between symbols and filling the gap using CP on the transmitter side after the IFFT. The cyclic prefix is removed on the receiver side on the time domain before the FFT. The increasing length of the cyclic prefix because increasing time delay in the OFDM. The increasing delay has increased the power of all system and reduces the spectral efficiency due to the delay.

The OFDM baseband subcarriers are described as:

$$s(t) = \frac{1}{N} \sum_{k=0}^{N-1} X_k \phi_{k(t)} \quad (4.13)$$

$$\phi_{k(t)} = e^{-j2\pi f_k t}, \quad 0 < t < N \quad (4.14)$$

Where :

N: number of subcarriers equal to the length of OFDM symbols

X_k : subcarriers encoded

The subcarrier frequency f_k are equally spaced

$$f_k = \frac{k}{NT} \quad (4.15)$$

The Cyclic Prefix insertion is shown in the equation :

$$\varepsilon(t) - s(t) \quad \Delta < t < NT \quad (4.16)$$

The OFDM symbol in the equation (4.9) is extended over a period Δ [58].

The time duration of the OFDM symbol with CP is represented in the equation below:

$$T_{OFDM} = T_{sym} + T_{cp} \quad (4.17)$$

The cyclic prefix is added to the IFFT directly during the generation of an OFDM symbol which is available with Simulink Xilinx Pipeline-streaming_IO_FFT v8.0 natural order. The insertion CP means more samples are unloaded from IFFT IP core than loaded, but the core cannot continuously stream frames. The insertion must leave a gap for the CP by inserting a length of clock cycle between each symbol of input data to accommodate the additional clock cycles required for unloading CP. The output signal from IFFT **s_axis_data_tready** goes low to allow the IFFT time to unload CP. This signal is fed back to IFFT through the port of **s_axis_data_tvalid** input to allow the IFFT to receive new subcarriers when it is going active high. Moreover, the same signal is sent to the FFT on the receiver side **s_axis_data_tready** to remove CP and to process the OFDM symbol without CP.

The block diagram of the OFDM design model with the Cyclic prefix is described in **Figure 4-25**.

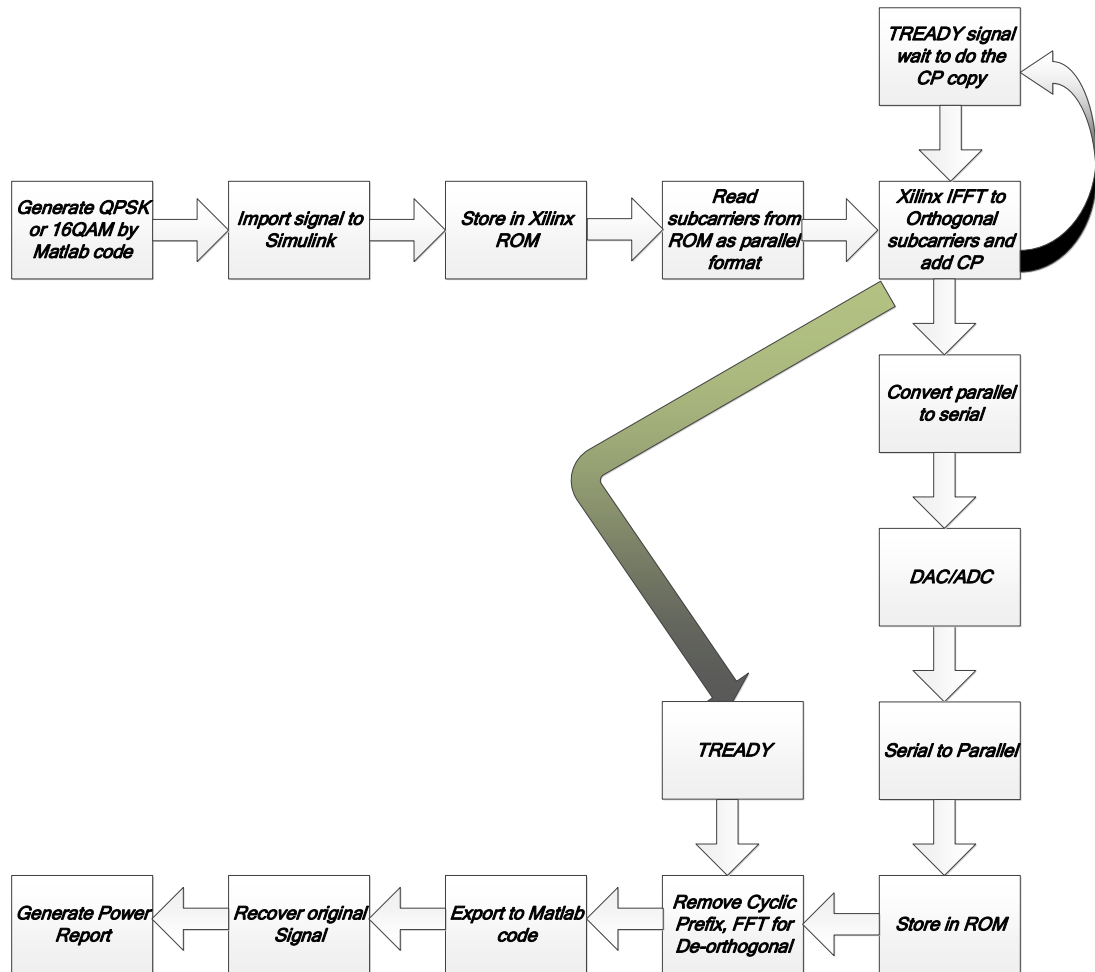


Figure 4-25 Block diagram of OFDM model with the location of CP

The location to add CP in the block diagram above is shown in the red box above the IFFT in the transmitter and the FFT in the receiver. The signal generated from the IFFT shows the process of generating CP and added to OFDM symbol. The setting of System Generator Xilinx IP core FFT Block which is used in the OFDM transmitter design model is described in

Figure 4-26. The IFFT includes an option of adding CP with the length of CP.

During the copy operation of the CP, the output signal from IFFT (TREADY) is going and use this signal as a feedback to IFFT to stop receiving data during the copy operation. The TVALID signal is used when IFFT ready to receive new subcarriers to process.

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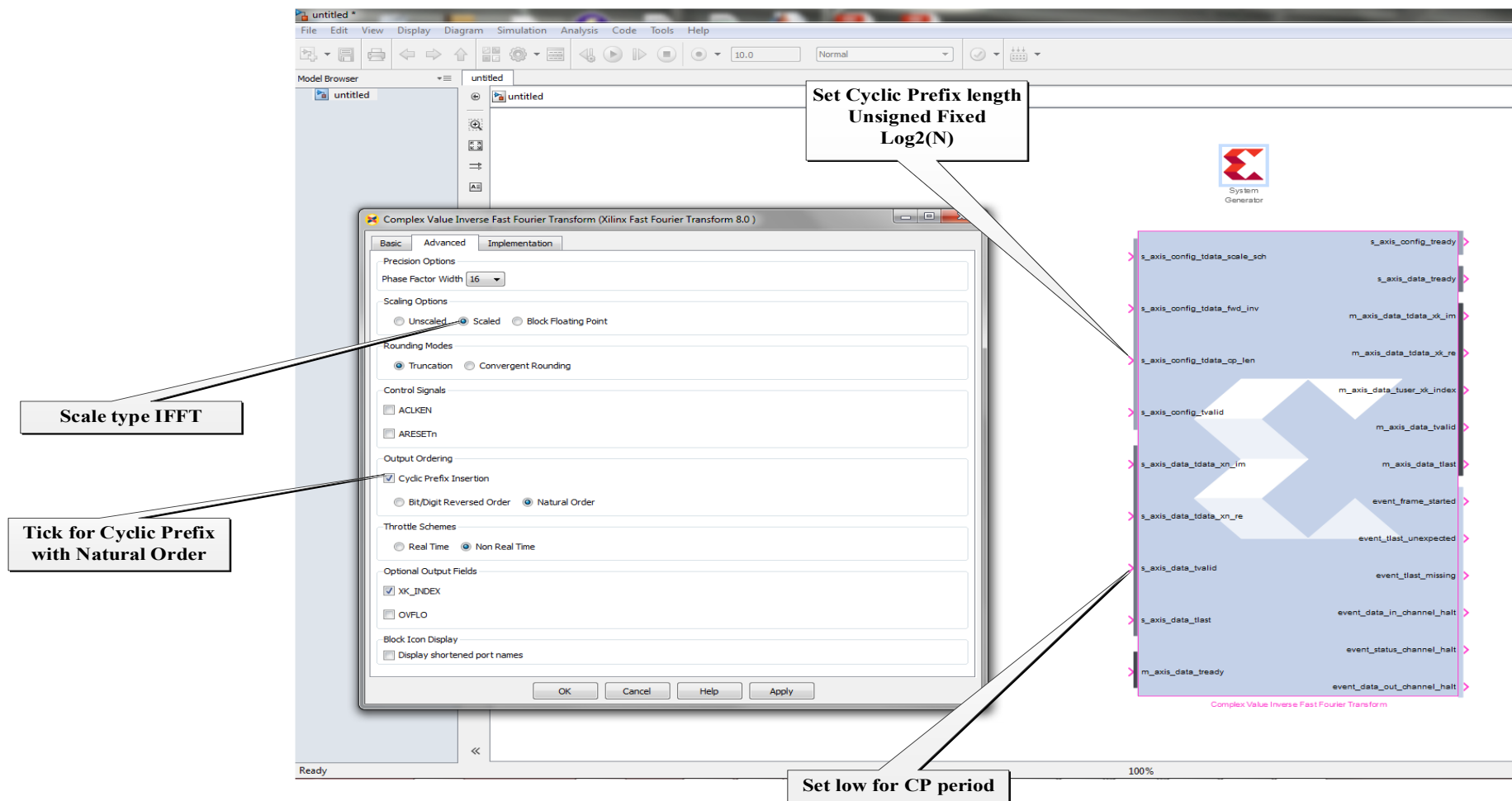


Figure 4-26 Setting of IFFT with CP

This section has researched about the effect of the CP and the FPGA power consumption of Xilinx IP core IFFT for the OFDM modulation. The two types of the subcarriers (16QAM and QPSK) are used for two OFDM model (complex and real) value IFFT.

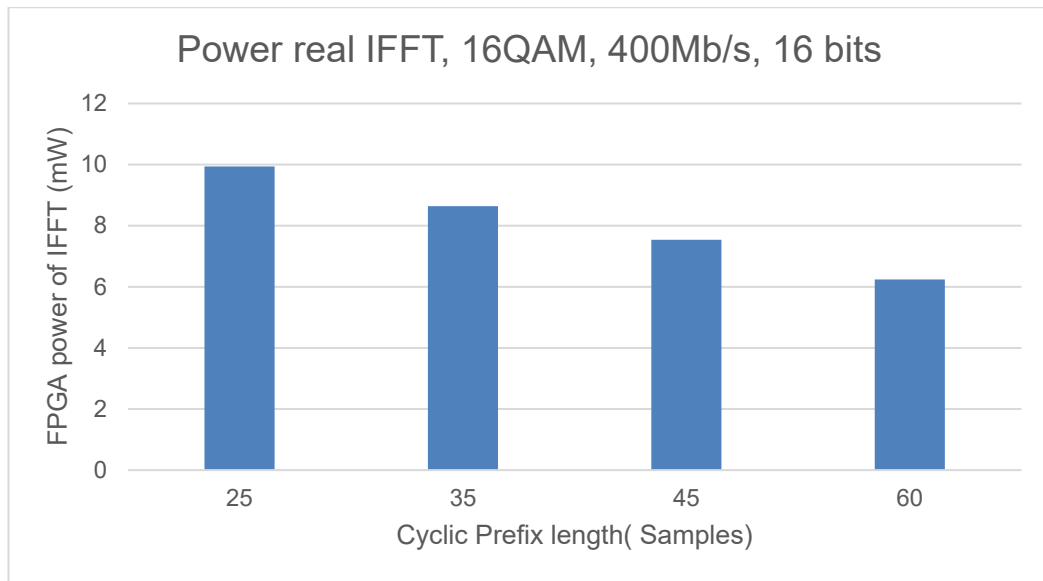


Figure 4-27 Real IFFT power diagram with different Cyclic Prefix length.

In this experiment has used a different length of Cyclic Prefix (25, 35, 45, and 60) subcarriers applied to real value IFFT. The subcarriers modulation uses 16QAM with a bit rate of the subcarrier of 400Mb/s and the precision calculation of 16bit. The result has found the FPGA power consumption on IFFT is shown in **Figure 4-27**. The results show that the FPGA power of IFFT is decreased when increasing the length of Cyclic Prefix inside of the OFDM symbol. The reduction power is 8% when increasing the CP from (25 to 35) and increase to 22% reduction in power consumption when CP 45 and to 31% decrease when increasing the CP to 60 cycles.

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This reduction because the IFFT is turned power OFF during a copy operation of CP. The copy duration comes from the output signal name `s_axis_data_tready` goes low during a copy operation for the CP.

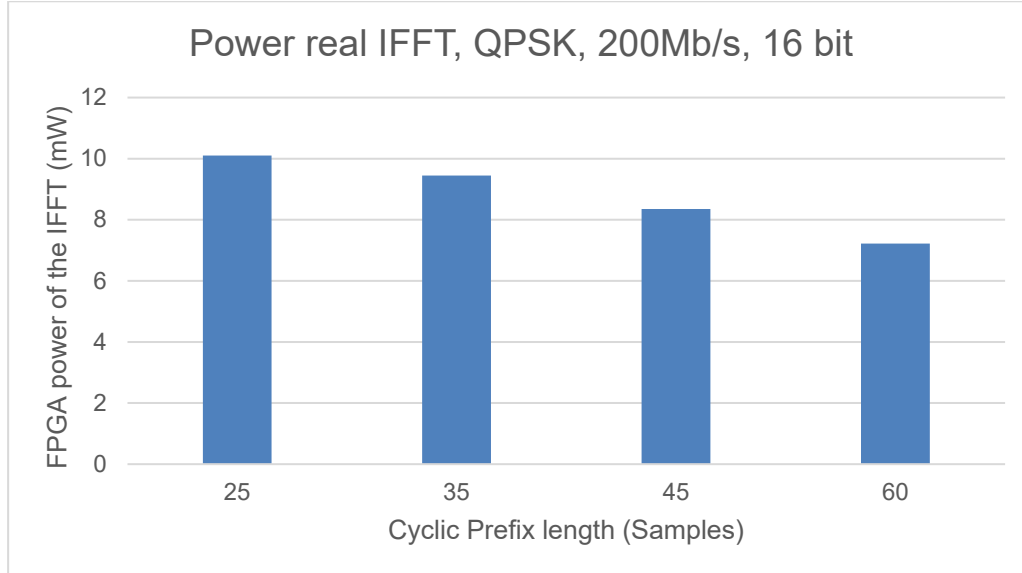


Figure 4-28 Real OFDM modulation with QPSK subcarrier and variant Cyclic Prefix

The second experiment is implemented with subcarrier encoded by QPSK and uses the same parameters setting of the previous experiment. The speed rate is 200Mb/s for this experiment and the sampling frequency 100Mhz. The result of the FPGA power consumption is shown in Figure 4-28 shows the power decreases with increasing cyclic prefix. The power reduction of 7% when increasing the CP from (25-35). The power reduction of the power consumption of IFFT is increased to 17% for CP length (25-45) samples. Finally when compared the FPGA power for the CP length from (25-60) samples the power is decreased by percentage 28%.

The increased length of CP samples led to increasing the space of the parallel data input to IFFT then reduce the processing inside the IFFT. Moreover, increases the period of Cyclic Prefix led to increasing the copy which means increasing the turn power OFF of the IP core IFFT during the

copy operation. The power is the total average power during generation the OFDM symbol with CP.

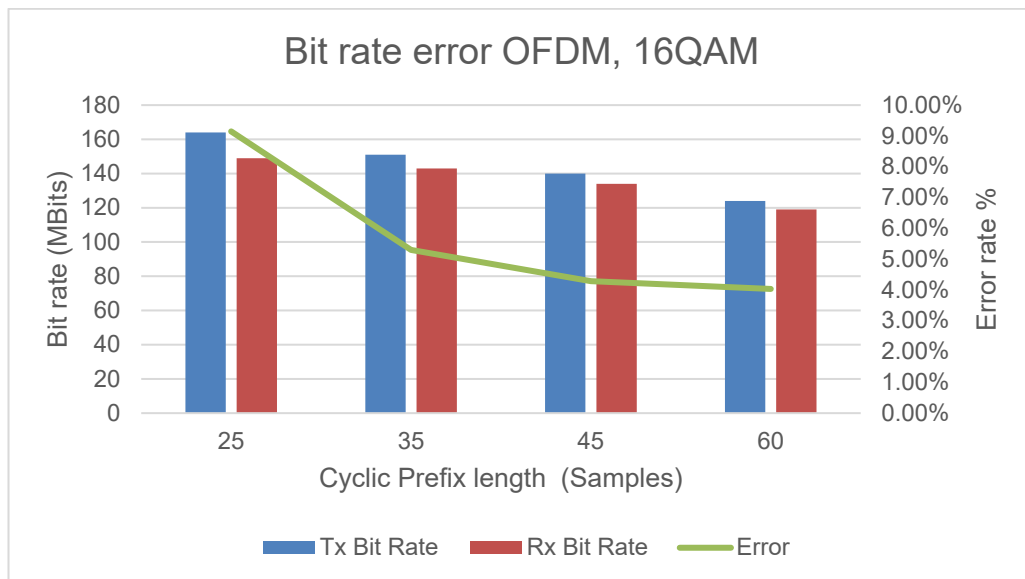


Figure 4-29 Bit error rate of real OFDM with Cyclic Prefix variant length

The bit error rate between the transmitter and receiver for OFDM model using 16QAM subcarriers is shown in **Figure 4-29**. The error is reduced with increases length of the cyclic prefix samples, and the bit rate is reduced with increasing length of the cyclic prefix. The error rate is 9% with 25 samples of the CP length and reduces to 5% with 45 samples of CP then to 3% error when select 60 samples of CP.

The Complex OFDM model is simulated to discover the effect of Cyclic Prefix on IFFT power consumption and the result is shown in **Figure 4-30** and **Figure 4-31** for two subcarriers types QPSK and 16QAM.

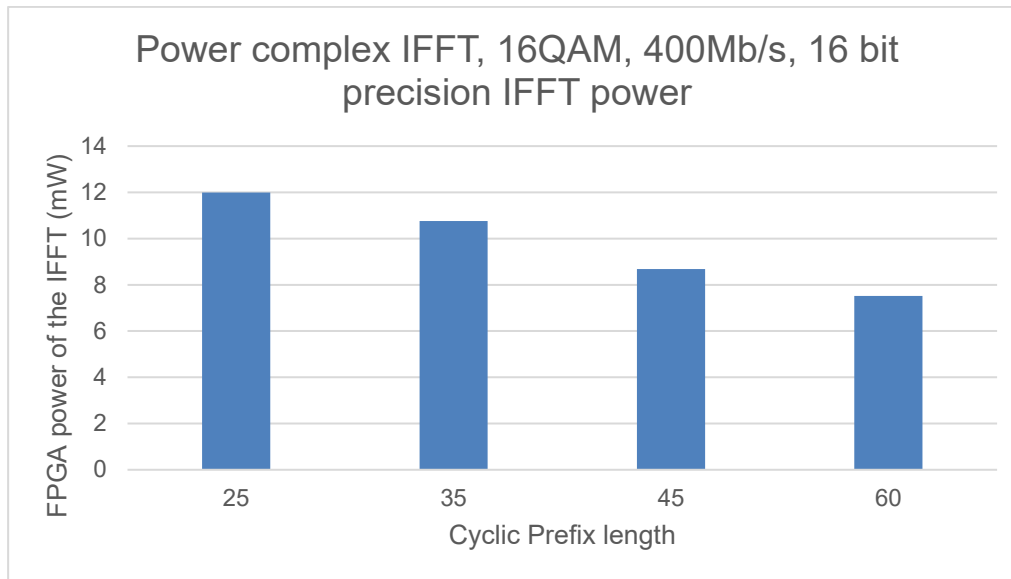


Figure 4-30 Cyclic Prefix effect FPGA Power of complex value IFFT

The effect of CP length on FPGA power consumption of complex IFFT for OFDM model by using 16QAM is shown in **Figure 4-30**. The figure shows the power of IFFT in a column for each length of CP selected. The result compares the percentage change in the IFFT core power consumption with increasing the CP length. The reduction power by 10% when the CP increased from (25-35) samples. The increasing length of the CP from (25-45) the power consumption reduced by 25%, and this percentage increases to 38% with CP length increase from (25-60) samples. The percentage had compared the reduction in power consumption of IFFT with CP 25 sample length.

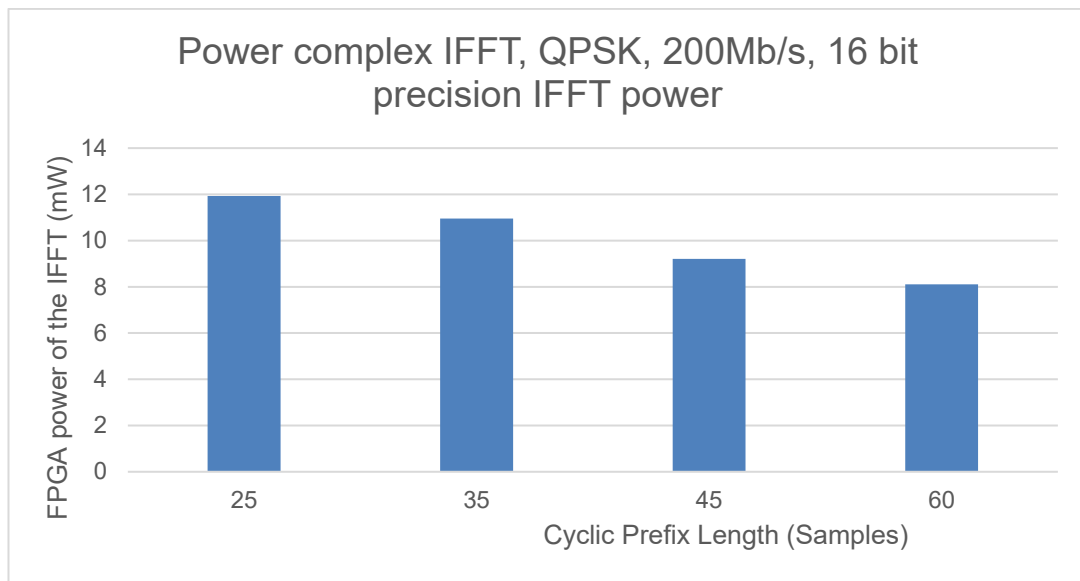


Figure 4-31 Cyclic Prefix Effect on QPSK of Complex OFDM Power of IFFT

The different subcarriers modulation uses to find the effects of CP length on FPGA power consumption of the IFFT. In this experiment uses QPSK subcarriers to generate the OFDM symbol. The result shows that the FPGA power of the IFFT is decreased with increasing the length of CP. The CP increases from (25-35) sample the power decrease by 8% and increases to 22% when increasing the CP length from (25-45) samples. Finally, the power reduces to 32% when increasing the CP length from (25-60) samples.

The experiments implemented above compare the FPGA power of the IFFT with the effect of increasing the length of CP. The power reduction because the copy operation inside Xilinx IP core IFFT which is reduced the processing of the orthogonal subcarriers. The average FPGA power of IFFT is reduced when increasing CP length because of stop processing operation during the copy of the CP.

4.7 Length of IFFT/FFT

The IFFT is the important part in the OFDM transceiver which is responsible for the orthogonality between the encoded subcarriers. The input to this part is a parallel encoded subcarrier equal to the length of IFFT, and the output is an OFDM symbol. The length of IFFT can be identified by the length of the OFDM symbol after the IFFT, according to the design model.

The increasing length of IFFT required more subcarriers to feed it which led to increasing

- Number of point input.
- Power consumption.
- Occupied large chip area.
- Number of the stage inside IFFT.
- Number of processing calculations.
- The length of ROM before IFFT.

The number of stages for Radix2 butterfly is calculated as in eq (4.18) :

$$\text{Number of stages} = \log_2(\text{FFT length}) \quad (4.18)$$

Each IFFT/FFT stage is included $N/2$ butterflies where N is the length of IFFT/FFT. Each butterfly had a multiplication and addition as a mathematical operation.

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The length of the IFFT/FFT which increase the number of subcarriers input, internal structure, and the area used inside the FPGA.

The equation of the OFDM symbol including the subcarriers used is described in eq(4.19):

$$S_n = \frac{1}{N} \sum_{i=0}^{N-1} A_i e^{j2\pi \frac{i}{N} n} \quad n = 0, 1, 2, \dots, N-1 \quad (4.19)$$

The equation above is similar to the IFFT equation [40]. The N represents the number of subcarriers so increasing the N will increase the iteration summation \sum . This will increase the addition and the multiplication of equation above, which increases the FPGA power consumption of the IFFT.

The received data is recovered by FFT as described in the equation (4.20):

$$A_i = \sum_{n=0}^{N-1} S_n e^{-j2\pi \frac{i}{N} n}, \quad n = 0, 1, 2, \dots, N-1. \quad (4.20)$$

S_n : Received OFDM sample.

A_i : Received information symbol for the i th subcarrier

The experiment is implemented using 16QAM subcarrier modulation with a sampling frequency of 100Ms/s. The result found that the effect of IFFT length FPGA power consumption by comparing the different length of IFFT 128, 256, 512 points. Therefore, ROM is used to store subcarriers in the parallel format before IFFT which affected by the IFFT length and increases ROM size from 128 to 512 cells. The block diagram structure of this experiment is shown in **Figure 4-32**.

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The increasing length of the IFFT will increase the length of the frame input subcarriers and increase the length of the OFDM symbol generated. Furthermore, increase other components such as ROM size used to store subcarriers and OFDM symbol.

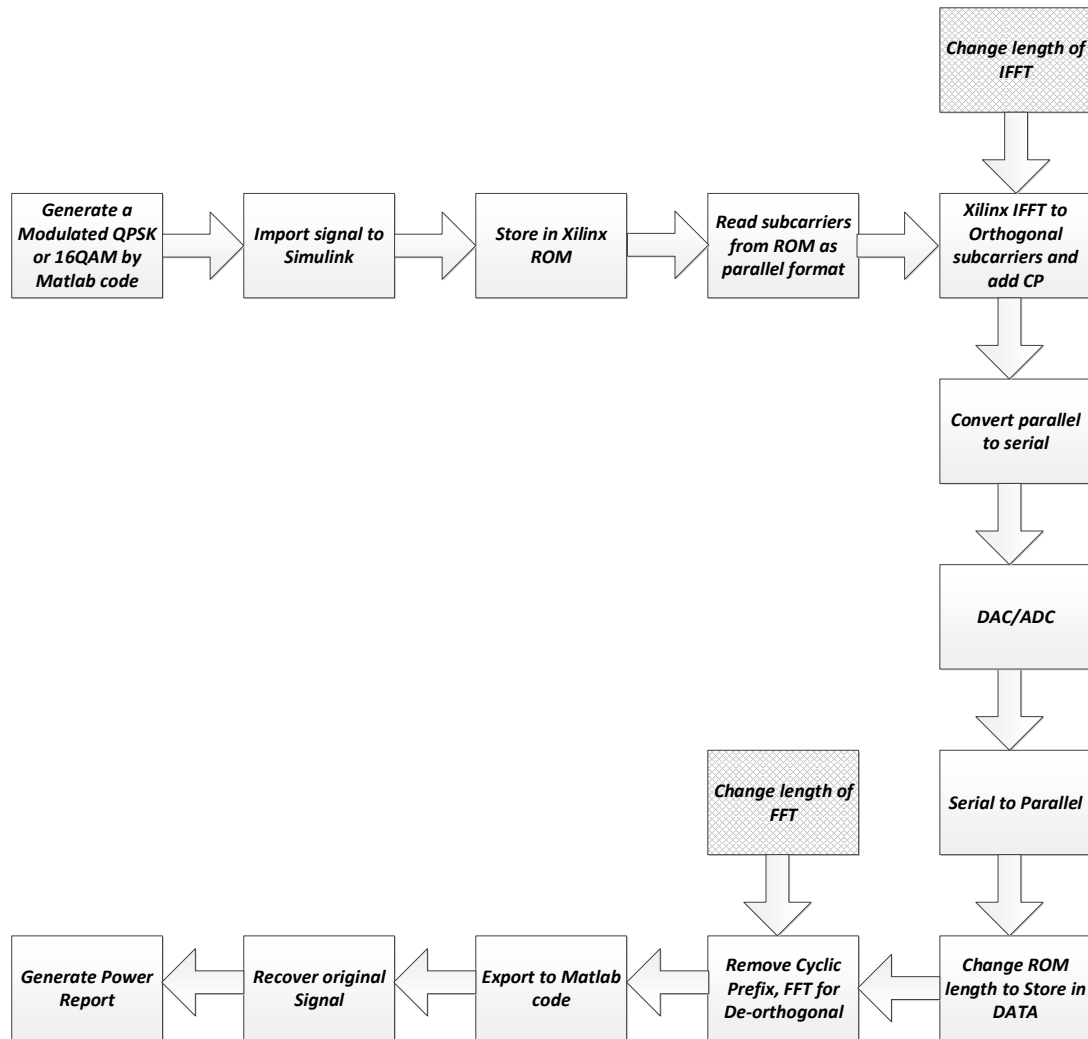


Figure 4-32 Block diagram of IFFT length Change

The red boxes in the block diagram show the location to select the length of IFFT/FFT. The FPGA power consumption result of the OFDM model design for one part IFFT in the transmitter side is shown in **Figure 4-33**. The experiment implemented on real and complex value OFDM by using a variable length of IFFT.

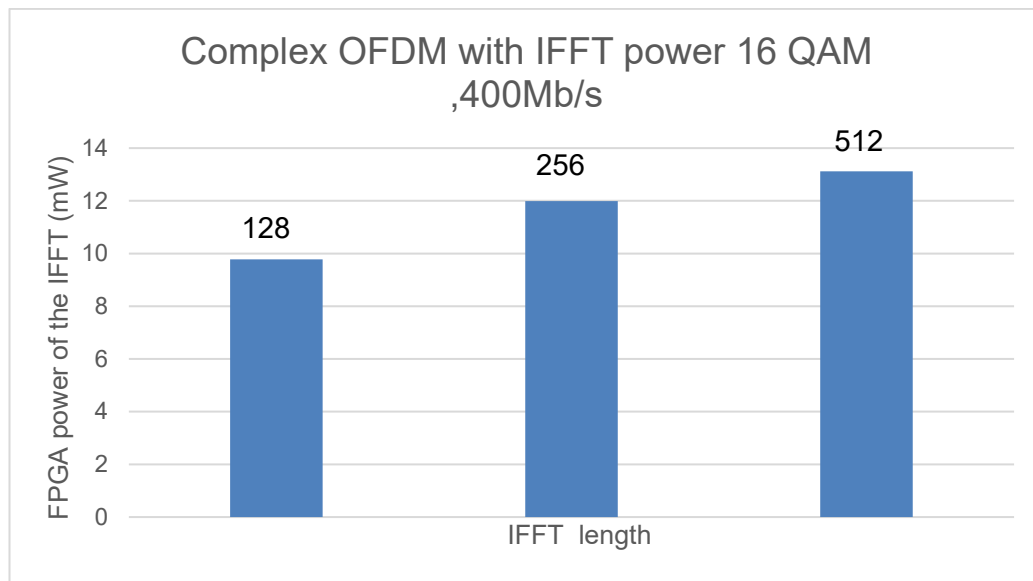


Figure 4-33 Power consumption with different complex IFFT length.

The increasing length of IFFT from (128-256) points led to increasing the power by 22.6% and increasing the processing subcarriers to double which is increased the OFDM symbol length. Furthermore, increasing the IFFT length from (128-512) points will increase the power by 34%. The advantage of increasing length of the IFFT is increase the length of the OFDM symbol generated but increase the FPGA power consumption of this part.

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The IFFT length effect on Real OFDM as a result shown in Figure 4-34

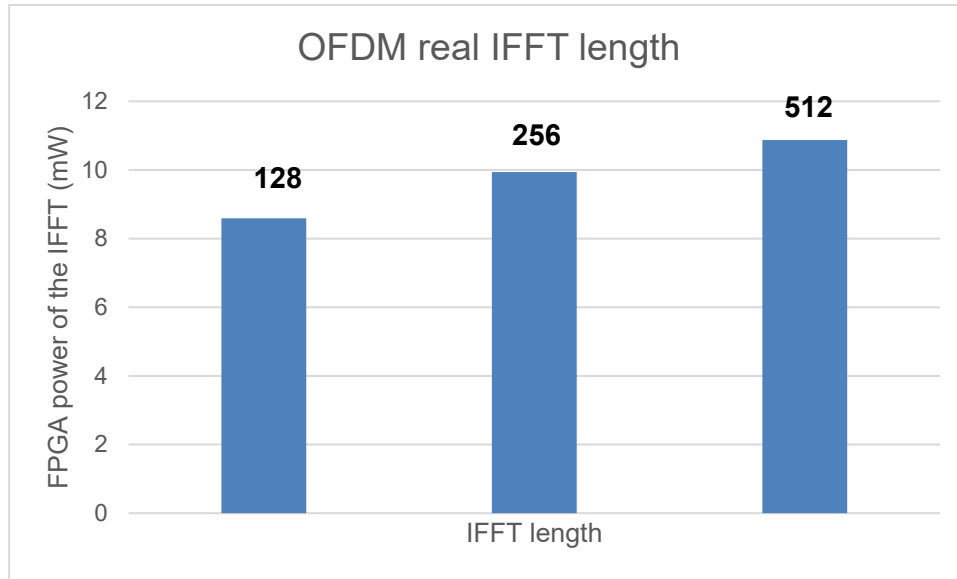


Figure 4-34 The IFFT length effect on Real OFDM

The result in the graph above shows the power increased with increasing the length of the IFFT. The discussion of the power increased as a percentage shows that the increasing length from (128-256) will increase the power by 15.75 %. When increasing the length from (128-512) points will increase the power by 26.54%.

The increasing power depends on the number of the stages used in the calculation and the length of IFFT. The increase is due to increasing the number of inputs to IFFT which lead to an increase in the number of stages. The large size can improve the resistance to ISI and the BER performance of optical OFDM [7].

The result shows that the power between the complex and real value the percentage of increasing power for real value is lower than the complex value for the same length IFFT.

The percentage error rate is improved with increasing length of IFFT as in

Figure 4-35.

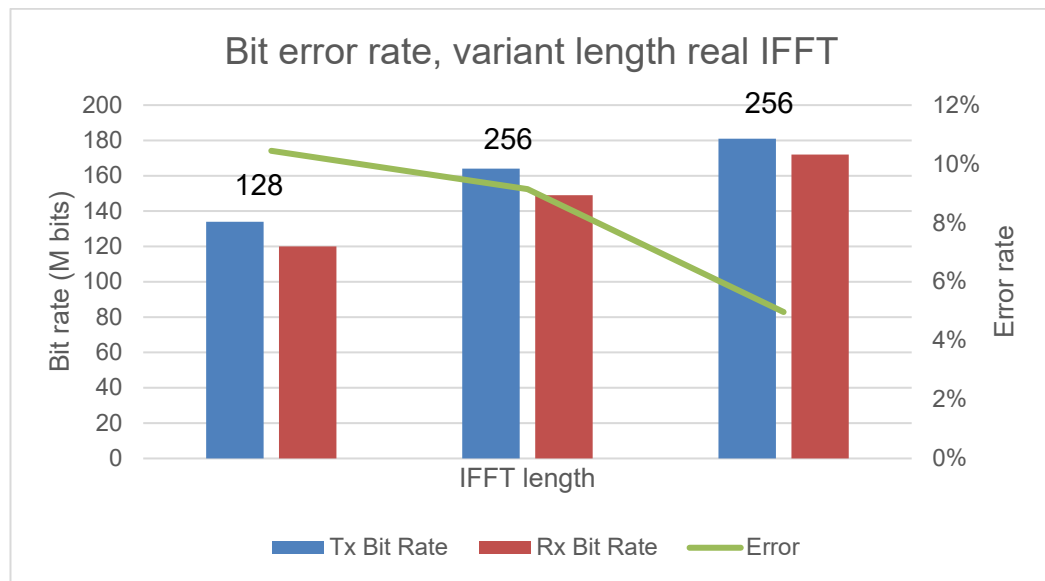


Figure 4-35 Error Rate of OFDM with variant Real IFFT length

The figure shows the error rate is decreased with increasing the length of IFFT which is 10.4% when using 128 lengths of the IFFT. This error is reduced when increasing the length of IFFT to 256-points, and the error rate is reduced to 9.2%. Finally, when using 512-points IFFT, the error reaches 4.9% with increasing the bit rate significantly higher than when using 128-points IFFT.

The power is increased with increased length of IFFT which will increase the length of the OFDM symbol and reduce the error between the transmitted and received signal.

4.8 Subcarrier Sampling frequency

This section has investigated the effect of the subcarriers sampling frequency on FPGA power consumption of the IFFT inside the OFDM model. The experiment is implemented with two sampling frequency (50-100) MHz for two subcarriers modulations type QPSK and 16QAM feed to the IFFT.

The number of bits transmitted over the OFDM symbol depends on the following parameters:

1. Sampling frequency
2. Cyclic prefix length
3. Subcarriers modulation types
4. IFFT length.

The previous section discussed the bit rate calculation of the OFDM symbol as in equation (4.21):

$$\textbf{Bit Rate} = \frac{\textbf{Number of bit per OFDM symbol}}{\frac{N_{FFT}}{f_s}(1+CP)} \quad (4.21)$$

In this section has discussed the subcarriers sampling frequency related to the OFDM data rate and the IFFT power consumption. The subcarriers bit rate is affected by subcarriers sampling frequency in modulation as in the block diagram of the design described in **Figure 4-36**.

The changing sampling frequency occurs inside the Matlab code when generating the subcarriers. It is shown in this figure with different colour blocks to represent the location of changing the sampling frequency.

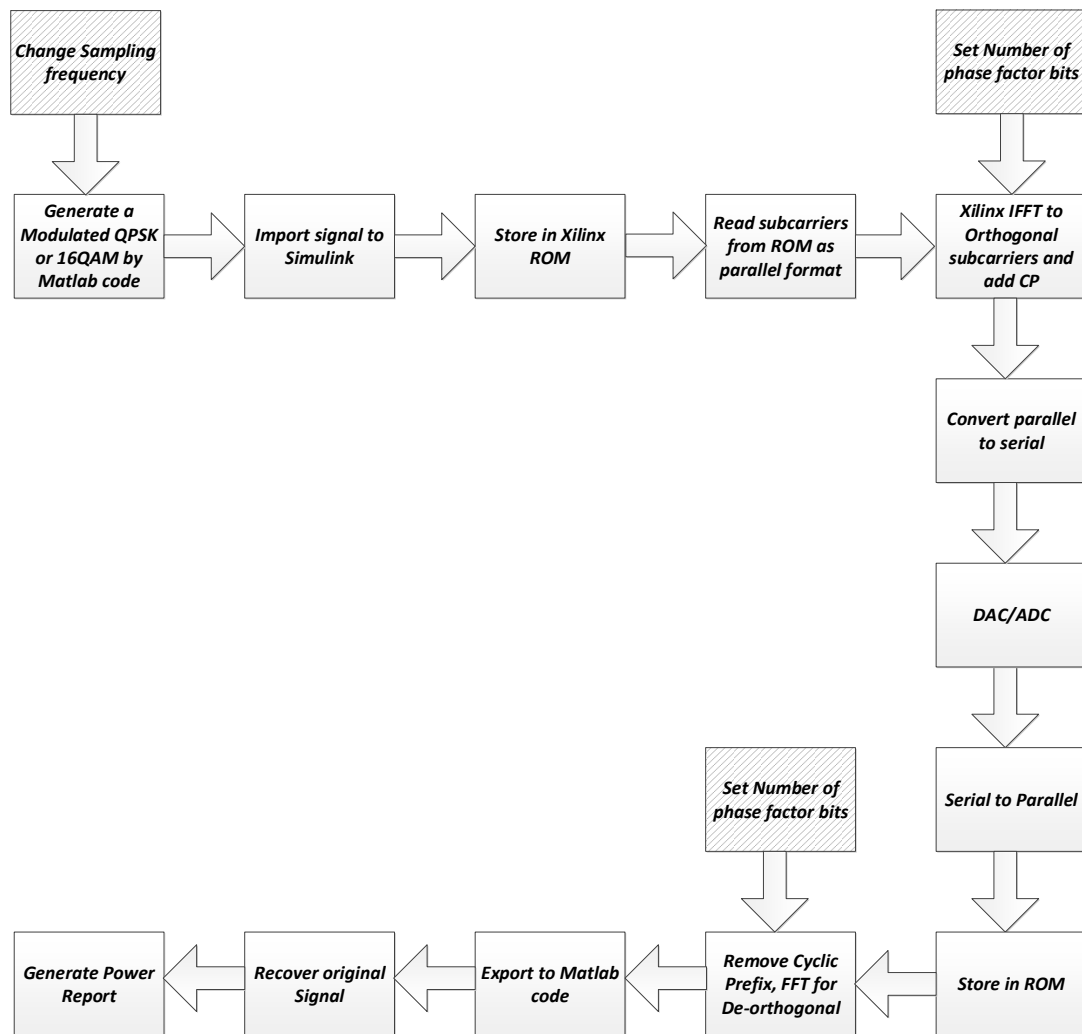


Figure 4-36 Block diagram of the sampling frequency of OFDM

There are two experiments implemented for different sampling frequency, and different numbers of bit precision phase factor use with real value IFFT.

The first model uses 16QAM subcarrier modulation feed to IFFT with two sampling frequency (50-100) MHz Each subcarrier carries 4 bits with bitrate (200-400) Mb/s respectively. The phase factor bit precision varies between (10 to 32) bits and the output result is shown in **Figure 4-37**.

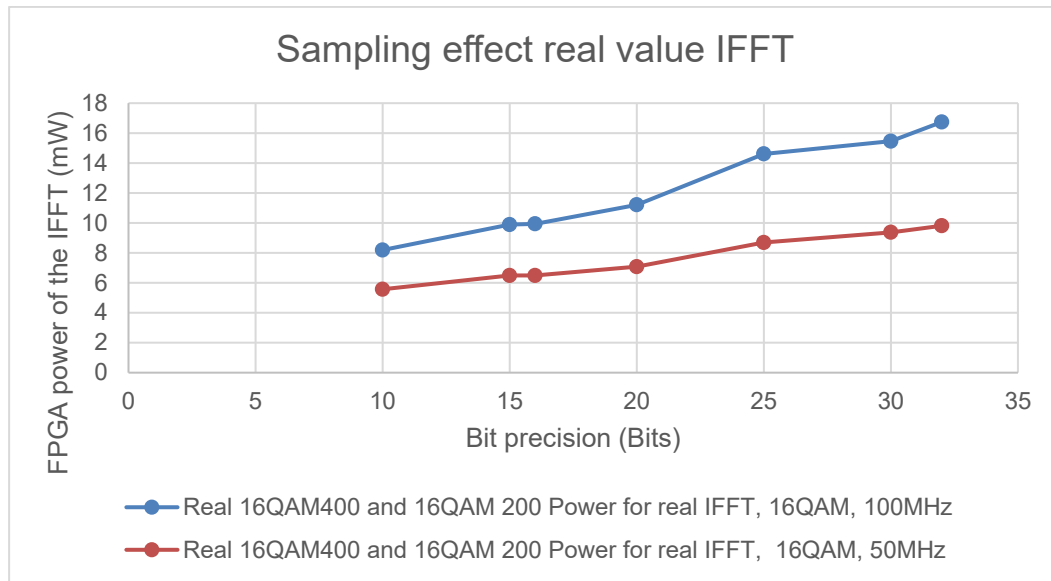


Figure 4-37 Sampling frequency effect on FPGA power of OFDM with 16QAM

The result shows the FPGA power consumption of IFFT has increased with increasing the sampling rate for same subcarrier modulation format. The experiment is implemented with 16QAM modulation. The sampling frequency increased from (50-100) MHz will increase the power by 47% for bit precisions 10 bits. The increasing bit precision to 20-bits the power increased by 58% and the average increase for all bit precisions from (10-32) is 60% increase. This increase is due to increase the bit per subcarriers or increase the bandwidth of the subcarrier input to IFFT.

The experiment is implemented with QPSK modulation type and uses two sampling frequency 50 and 100 MHz. The result compares the two sampling rate frequency for the real value OFDM is shown in Figure 4-38.

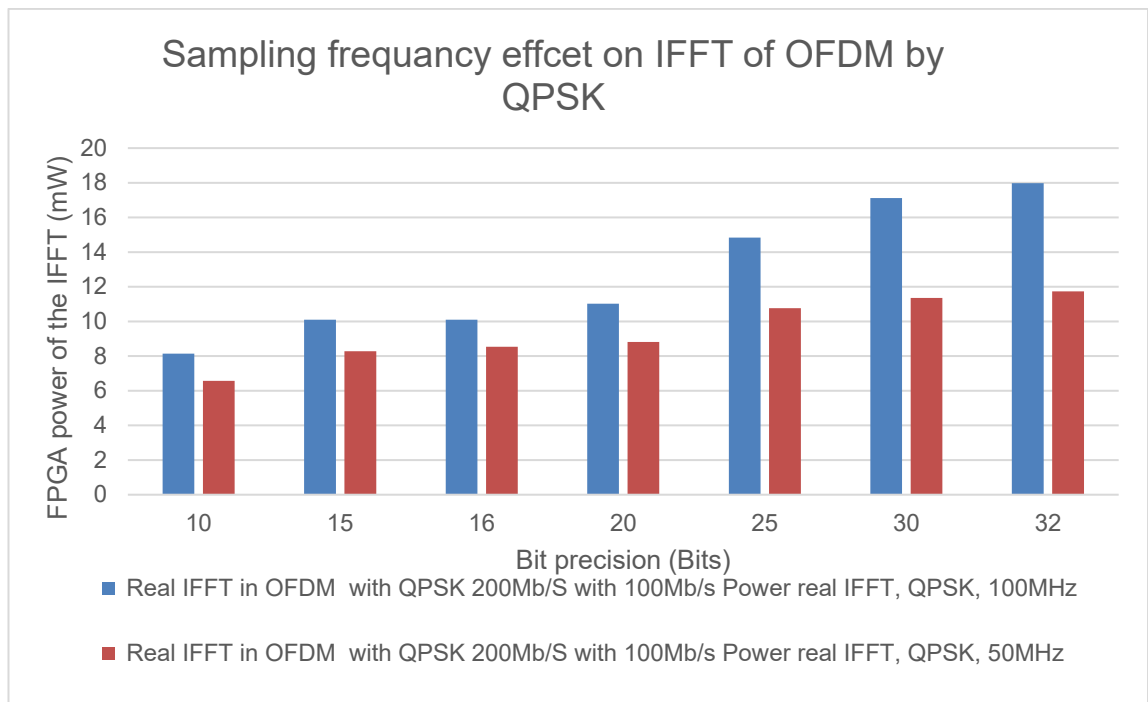


Figure 4-38 Power consumption of Real value OFDM with QPSK and variant speed.

This experiment uses the same setting used in the previous experiment with sampling frequency change from (50, 100)MHz of the QPSK subcarriers. However, the QPSK bit rate is (100, 200)Mb/s because QPSK carries 2 bits per subcarriers. The power measurement of the IFFT shows that the power is increased by 24% when increasing sampling frequency from (50,100)MHz with 10-bits precision. The increasing bit precisions to 32 bit the power is increased by 53.28% for two different sampling frequency. The average increase by 33% for the FPGA power consumption of IFFT with a different sampling frequency of the subcarriers.

The complex IFFT uses QPSK as an input subcarriers to generate the OFDM symbol for different sampling frequency has implemented an experiment and the result is shown in **Figure 4-39**.

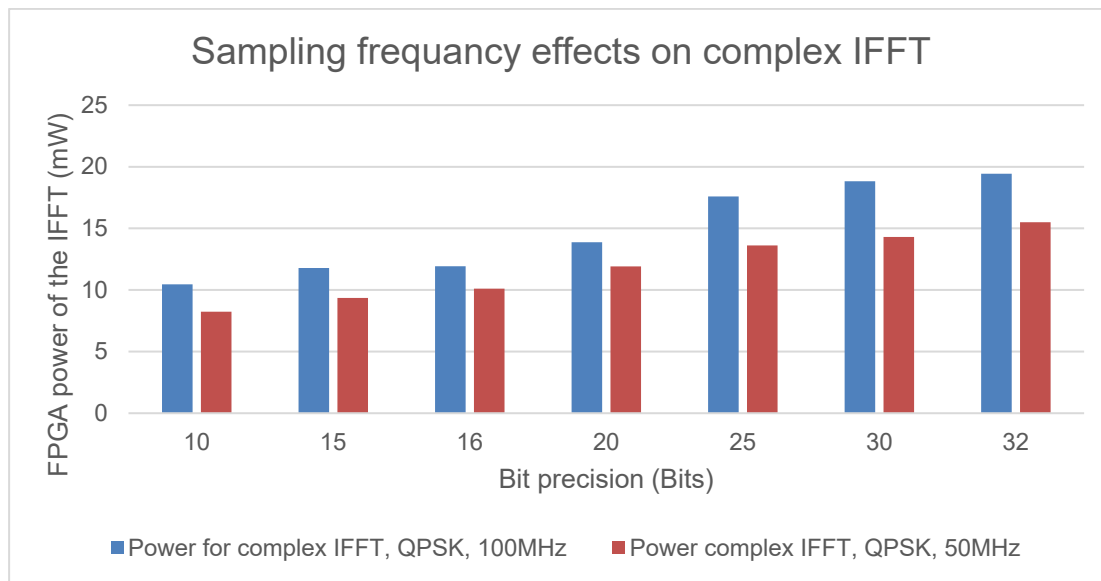


Figure 4-39 Sampling Rate Effect on Power of complex IFFT in OFDM

The result shows the FPGA power is increased with increasing sampling frequency. The power is increased by 22% with 10-bit precision and the sampling frequency between (50-100)MHz. The average increase in the power consumption of IFFT for all bit precision of the experiment above is 25%.

In the summary, the sampling frequency is effected the complex and real value IFFT power consumption in FPGA by increasing the FPGA power consumption when increasing the sampling frequency for both real and complex value IFFT and different subcarriers modulation type.

4.9 Subcarriers Modulation

This section discusses the effect of the modulation type on FPGA power consumption of IFFT in OFDM. The OFDM modulation uses a basic subcarrier modulation such as QPSK or different level of QAM modulation to carry data. The subcarrier modulation effect on FPGA power consumption of IFFT used in OFDM is discussed in this section.

In OFDM, uses the IFFT to generate the OFDM symbol by orthogonal the subcarriers input. The FFT is used in the receiver to De-Orthogonal the OFDM symbols and recovery the original signal. The increasing number of bits per subcarriers by changing the modulation types will increase in the processing operation inside the IFFT and generate long OFDM symbol. The increased number of bits used to represent the subcarrier which depends on the modulation type. In QPSK uses 2 bits per subcarrier which is four states (00, 01, 10, 11) but when uses K-QAM the number of bit per subcarrier is $\log_2(K)$ bits where K represents the data subcarriers order. The processing of the IFFT is increased with increasing number of bits per subcarrier.

The block diagram of the various modulation types of the OFDM design used in this experiment is shown in **Figure 4-40**. There are three different colour block which is show the location of selecting the modulation type and affected the design with power consumption of IFFT/FFT.

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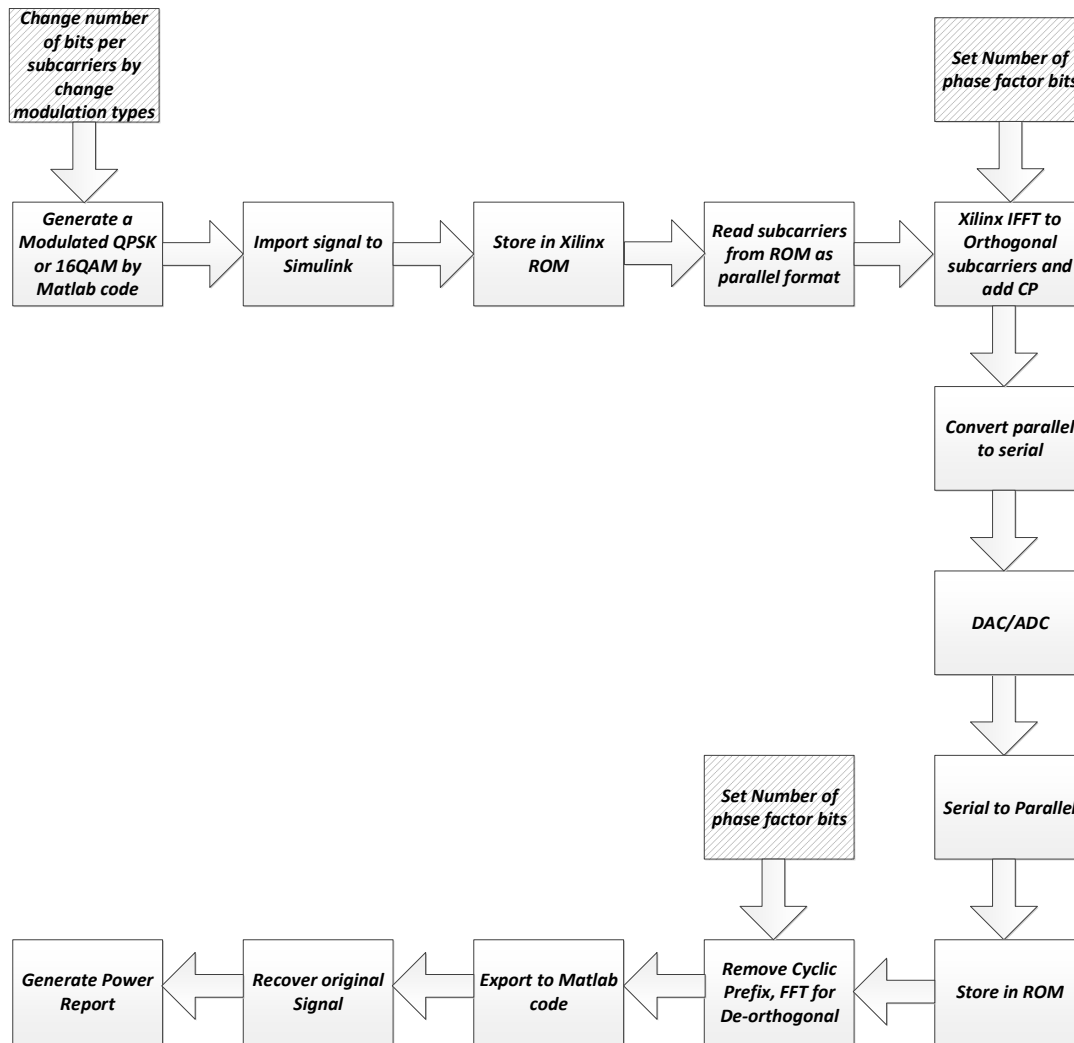


Figure 4-40 Block diagram of the effect of modulation type on IFFT/FFT power.

The block diagram in the figure above shows the location to select the subcarriers modulation types with different colour box and occurs in the first block in Matlab code when generating the subcarriers. This section compares the IFFT power consumption in FPGA of real and complex value OFDM model with two different subcarriers modulation techniques: QPSK and 16QAM. The first experiment, compares the FPGA power consumption on the real value IFFT uses the same bit-rate 200Mb/s for both modulation types. The result of the experiment is shown in **Figure 4-41**.

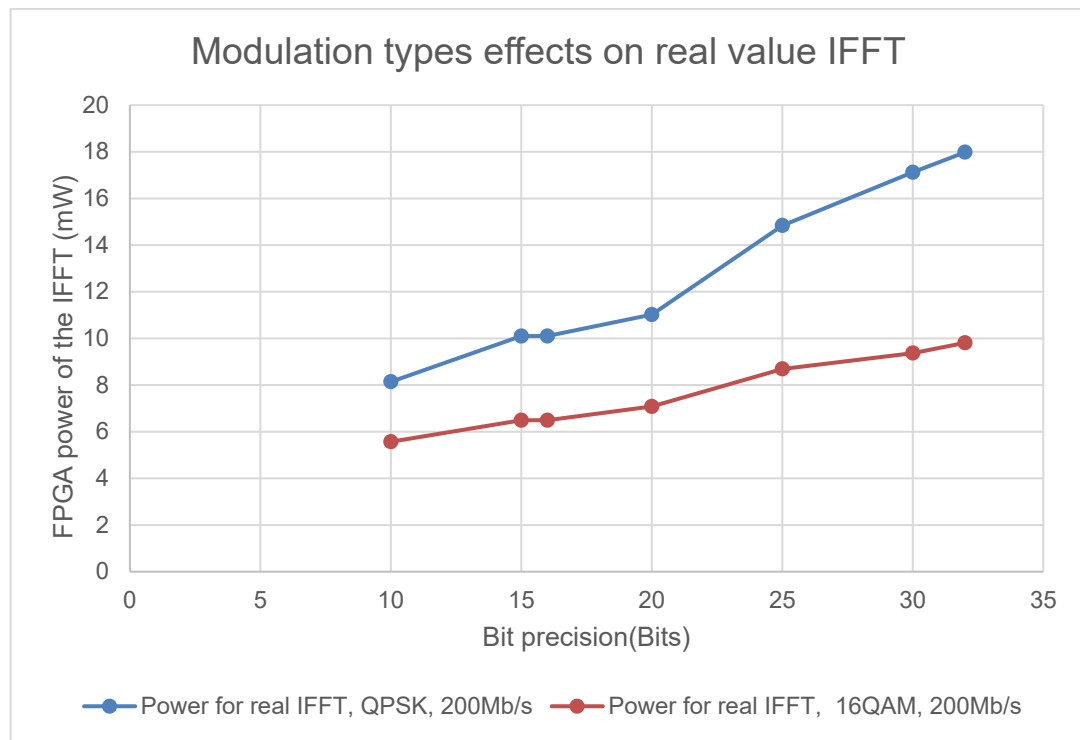


Figure 4-41 OFDM model with IFFT power and different subcarrier modulation

The result in **Figure 4-41** above shows the 16QAM subcarriers feed to IFFT and consumes lower FPGA power when compared with QPSK subcarriers at the same speed with a different number of phase factor bit precision. The FPGA power of IFFT has decreased by 31% for 10-bit precisions. This increases with increasing the bit precisions to 46% reduction on FPGA power with 32-bits. The average power reduction for 16QAM compared with QPSK of all the experiments is 38%.

Comparing the result of the power consumption of real value IFFT with different subcarrier modulation types (QPSK, 16QAM) with the same sampling frequency of 100MHz and bit precision of 16-bits the result is shown in **Figure 4-42**.

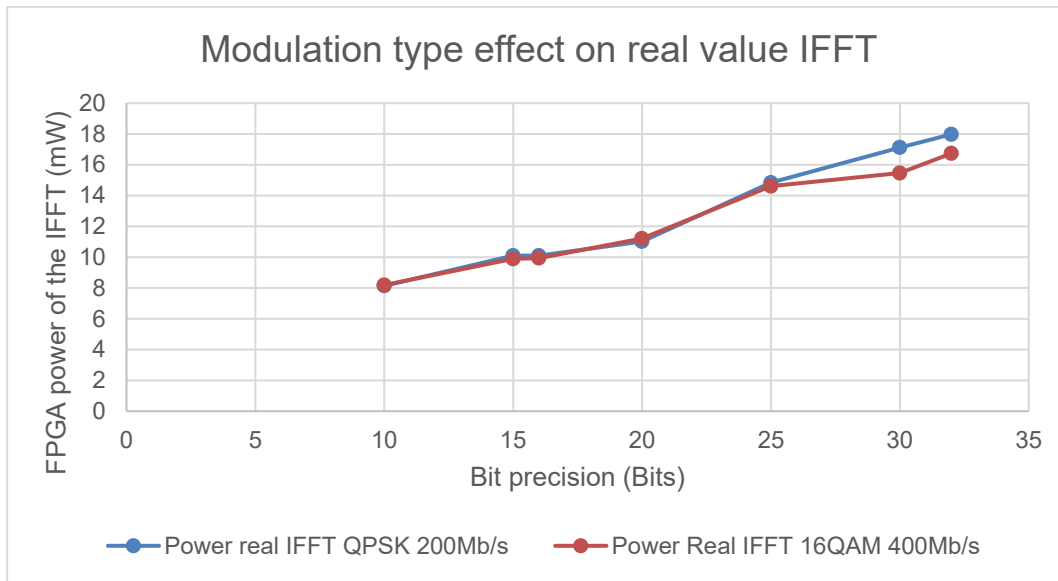


Figure 4-42 Power consumption Real IFFT for different modulation

The figure above shows the real value IFFT power consumption is approximately the same for both 16QAM and QPSK by using same sample frequency for both cases. The small difference in power consumption between QPSK and 16QAM. The percentage decrease is 0.61% for 10 bits, and increase to arrive at 7% decrease for 32-bit. The average difference reduction is 3.5% for the experiment above. The bit rate for 16QAM is higher than in QPSK by double for the first case 400Mb/s and QPSK 200Mb/s but consumes approximately the same power in both cases.

The result is compared the FPGA power consumption of the complex value IFFT use in OFDM. The setting parameters uses QPSK with 200Mb/s and 16QAM, 400 Mb/s, and sampling frequency 100MHz. The result of the power consumption is shown in **Figure 4-43**.

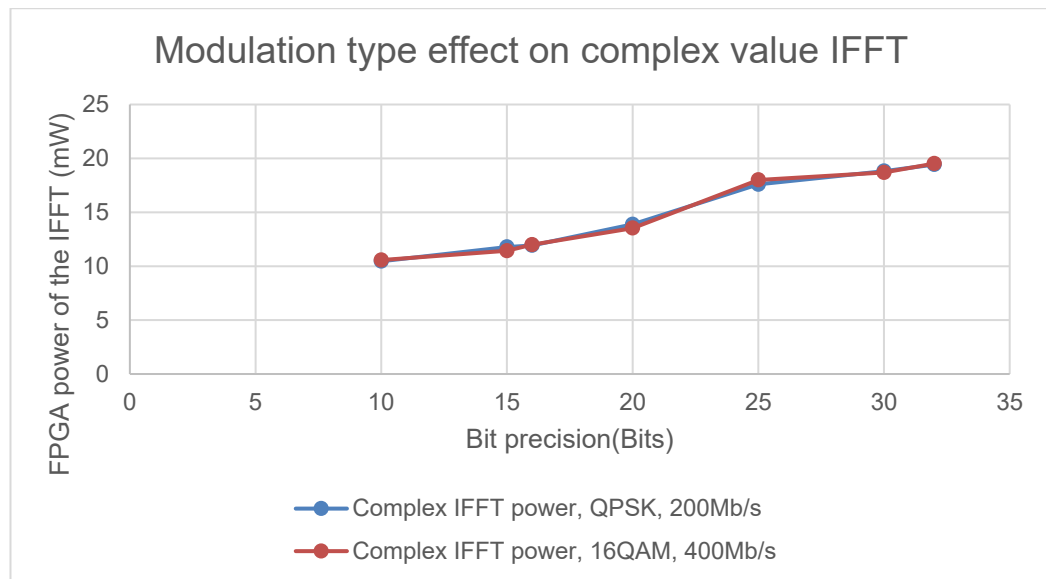


Figure 4-43 *Complex IFFT Power with different modulation*

The power is decreased by a percentage of 1.5% when using 10-bit precisions, and the average difference is 2%. The FPGA consumption power of IFFT approximately the same power of complex value when using subcarrier modulated by QPSK and 16QAM with the same sampling frequency.

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4.10 *Word Length Width*

This section discusses the effect of the word length bits width size on FPGA power consumption of the IFFT in the OFDM design model. The subcarriers are represented by a number of bit in a computer program which called the word length width(fixed and floating). This model is implemented with fixed bits type mathematical representation of the subcarriers, and the number contains two parts (integer and fraction) with the number sign.

The block diagram of the design model of the mathematical representation of word length bits width is shown in **Figure 4-44** which includes the location for selecting the different word length bits width size of the subcarriers.

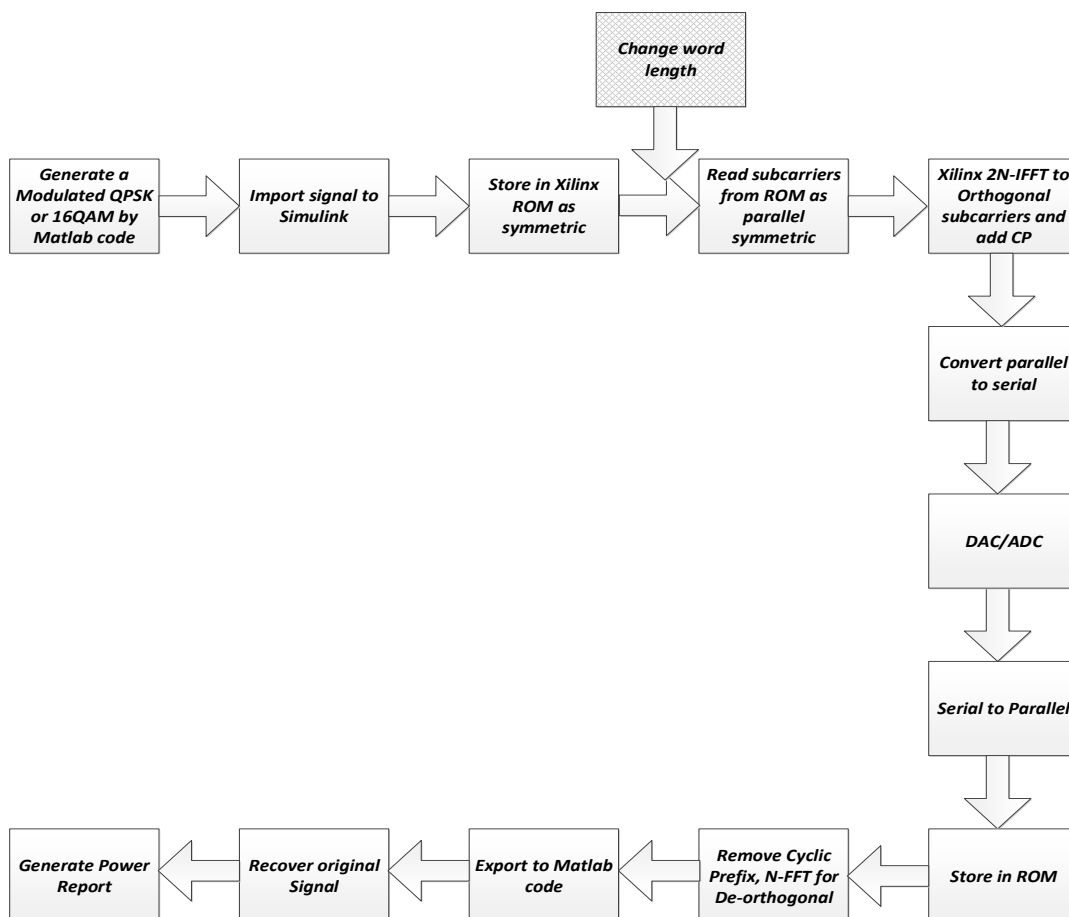


Figure 4-44 Block diagram of OFDM with various word length.

The red colour box before IFFT represents the location to select the width of word length used to a mathematical representation of the subcarriers. This experiment is implemented for OFDM model with the mathematical representation for the subcarrier by the word length bits width size fix16-15. This experiment finds the effect of reducing the word length bits width and the FPGA power on IFFT.

It uses the real value IFFT with subcarriers modulated by QPSK and 10 bits precision phase factor, 200Mb/s speed, and sampling frequency of 100Mhz. The result of IP core IFFT power consumption is shown in **Figure 4-45**.

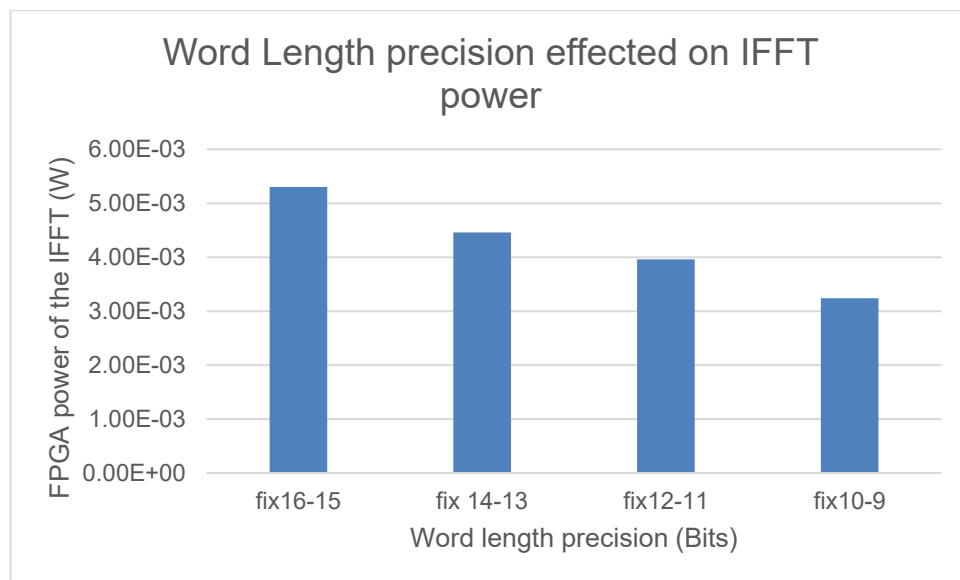


Figure 4-45 Word length width effect on IFFT power consumption

The results show the FPGA power of the IFFT in the OFDM model is decreased by reducing the word length size of the subcarriers. The power 5.3mW of IFFT with word length fix16-15 and the power decreases with decreasing the word length width to reaches to 3.24mW with a fix10-9 word length width.

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The FPGA power is divided into two parts logic, and signal power inside IFFT with the number of the components used inside the IFFT is shown in **Table 4-1** and **Table 4-2** below:

Table 4-1 Word length size effect on the FPGA power for the IFFT

Type	Fix16-15	Fix14-13	Fix12-11	Fix10-9
IFFT power(mW)	5.3	4.46	3.96	3.24
Logic(mW)	2.86	2.46	2.13	1.65
Signal(mW)	2.44	2	1.83	1.59

Table 4-2 FPGA components affected by the word length mathematical precisions

Type	Fix16-15	Fix14-13	Fix12-11	Fix10-9
FF	3031	2756	2482	2209
LUT	1752	1569	1421	1278
SRL	1110	1000	890	780
CARRYs	212	190	182	160

The two tables above includes all the hardware components inside the IFFT which are affected by the word length mathematical precisions. The decreasing word length size will reduce the FPGA power of the logic and signal inside FPGA components building the IFFT. Moreover, the mathematical precisions of the subcarriers word length bits width effect on the number of components build the IFFT by reduces the number of a component such as Flip-Flop (FF), a Lookup table (LUT), Shift Register Logic (SRL), and carry block.

4.11 Schemes comparison

This section has compares the researched parameters implemented in the previous section effected on the FPGA power consumption of the IFFT/FFT used in the OFDM model. The proposed model which produces the real value IFFT is used in the design of the real value OFDM transceiver with two location real only and the imaginary part equal to zero $X(0)$ and $X(N/2)$. The conventional OFDM is used for the complex value OFDM symbol uses complex value IFFT. The two types of subcarriers modulation (QPSK and 16QAM) are used in both OFDM model.

The result is compared between complex and real value IFFT and shows that the real value IFFT lower FPGA power consumption when compared with complex IFFT. The result shows that the average reduction in FPGA power of real value is 17% when using 16QAM subcarriers input when compared with the complex value IFFT. The percentage of power consumption of real value IFFT reduced by 15% when using QPSK subcarriers input. The result means the real value OFDM symbol with QPSK is consumed more power than 16QAM.

The difference in power consumption because the real value IFFT type is feed by double up the real part, and conjugated the complex part with two location equal to zero. Therefore, the power consumption is reduced due to a reduction in the processing and number of input to the real value IFFT.

The IFFT also affected by the number of bit precision calculation. The FPGA power significantly increases by increasing the number of bit precision.

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The power increase for using a small bit (10-15) bits the percentage of power increase is 8%, and for (16-32) bits the power is increased by 60% for complex value IFFT. However, the power for the real value IFFT increases by 21% when the bit precision (10-15) bits and 41% with bit precision increase (16-32) bits. This increasing because the processing inside IFFT is increased with increases the bit precision calculation.

Furthermore, the modulation type effects on IFFT power consumption. The complex IFFT power consumption increase by 2% in FPGA power when the subcarriers use 16QAM instead of QPSK with the same sampling frequency, and for real value IFFT increased by 3.5%. The percentage increase means that the power in real value with different modulation format is reduced. The increases because uses 4 bit per subcarrier in 16QAM instead of 2 bit in QPSK, but the result of the bit rate is double in 16QAM to reach to 400MB/s instead of 200Mb/s for QPSK. In addition, increasing the CP length will reduce the total FPGA power of the real and complex value IFFT because the processing is reduced during the copy operation.

The size of IFFT effected the FPGA power consumption for the complex and real value IFFT. The length of the complex IFFT increase from (128-256) points the FPGA power increase by 23%.

The length of real value IFFT increased from (128 to 256) the power is increased by 16%. The power consumed with large size IFFT because the processing of double up the subcarriers size and increase the OFDM symbol length.

The sampling frequency has effected on the IFFT power consumption by increases the FPGA power of IFFT with increasing sampling frequency. The power increase of real value IFFT using 16QAM subcarriers with sampling frequency increase (50-100)MHz the power will increase by 60%, and for QPSK the power is increased by 33%. This increasing because increasing the subcarriers bandwidth input to the IFFT. The word length width is effected the FPGA power consumption of IFFT by reducing the power consumption with lower word length width used.

The FPGA power consumption of FFT part was discussed in this chapter. The FPGA power of FFT is reduced by 46% when using OFDM symbol generated by 16QAM, and this percentage is reduced to 40% when using the OFDM symbol with QPSK. The power consumption difference between real and complex value because of only one part (real part) of the OFDM symbol input to the FFT and set the imaginary equal to zero. The bit precision effects the FPGA power of FFT with increased the power by 22% for bit increase from (16-32) bits in complex value FFT. The power is increased for real value FFT with the same increasing bit (16-32) bits by 57% power increase. This increase because of increases the calculation precision inside the FFT.

4.12 *Recommended setting*

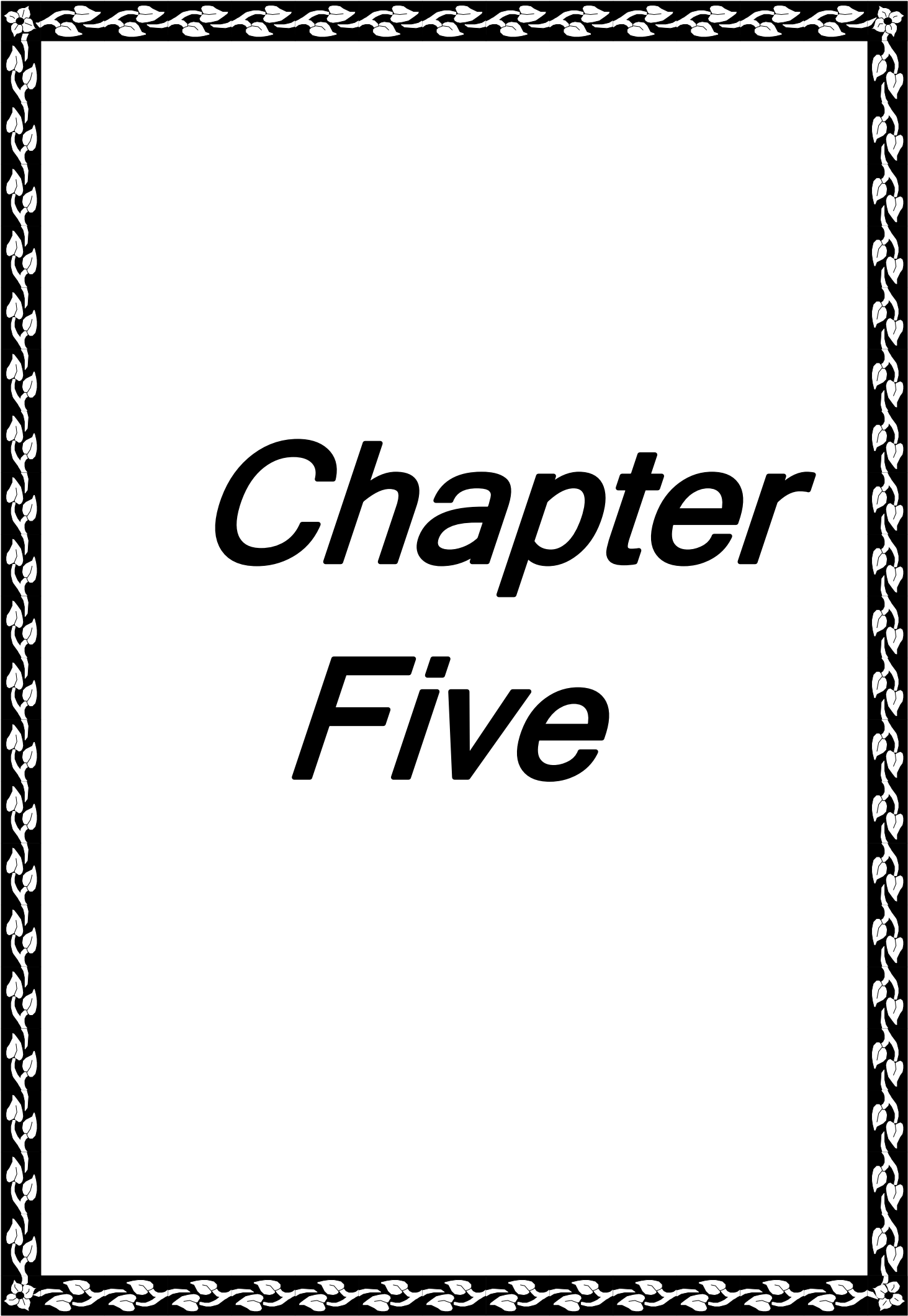
The recommended setting for the OFDM design included the researched parameters discussed in this section. The selecting real instead of complex value IFFT because of consumes lower power. The bit precision of IFFT selects the 16 bit because selecting lower bit precisions will reduce the power but error is increasing. The increasing bit precision will increase the consumed power by the IFFT. The CP length recommended is 10% from the subcarriers frame input to the IFFT. The selecting long length IFFT will increase the consumption power of it but increase subcarriers processing input and increase the length of the OFDM symbol output. In addition, high sampling frequency and high order modulation of the subcarriers are recommended for the design of the OFDM which increase the power but increase the bit rate and bandwidth to double but not increase the power to double. The recommended setting for the mathematical representation of the subcarriers bit precision called word length width depends on the recommendation of hardware user manual in this thesis recommended mathematical presentation Fix16-15 because included a DAC/ADC with the design.

4.13 *Summary*

The result presented in this chapter can be summarised as follows :

1. The description of the OFDM model built by using block diagram which is start from the software (Simulink Xilinx System Generator), the target hardware Kintex-7 evaluation board with high speed analogue DAC/ADC, and power generation report of the IFFT/FFT.
2. The setting parameters uses in the OFDM system setting such as symbol rate, subcarrier frequency, QPSK and 16QAM, bit rate, OFDM symbol duration, number of subcarriers used. This parameters setting are used for both models real and complex OFDM. In addition, the parameters setting of each Simulink Xilinx System Generator block used in the OFDM design.
3. The proposed model was explained in this chapter with the block diagram to identify the input type to IFFT. The subcarriers input is divided into two parts the part real part is double up, and the complex parts is conjugated with two location equal to zero.
4. The effect of the FPGA power consumption on IFFT/FFT for real and complex value OFDM had discussed. The Real value power consumption is lower than the complex value for IFFT/FFT for all subcarriers type QPSK and 16QAM. The real IFFT is lower power (10-20)% than complex IFFT and for the FFT Real value (30-50)% lower than complex value.

5. The precision calculation bit number used in the calculation of phase factor inside IFFT/FFT. The result shows that the power increased with increasing the number of bits used in the calculation phase factor.
6. The length of Cyclic Prefix samples effects on IFFT power consumption which reduces the power of IFFT when increasing the length CP.
7. The FPGA power consumption is increased with increasing length of IFFT/FFT. The increasing length will increase the number of subcarriers input to the IFFT and increase length OFDM symbol.
8. The effects of the subcarriers sampling frequency had increased the FPGA power consumption of IFFT with increasing sampling frequency of encoded subcarriers.
9. The subcarriers modulation type is effected on the IFFT power consumption. The power consumed by IFFT with 16QAM is lower than QPSK subcarriers, for the same bit rate in both experiments.
10. The mathematical bit precisions representation of subcarriers by word length width (number of bits) input to the IFFT had affected the FPGA power consumption. The increasing word length bit width had increased the FPGA power consumption.
11. Some of these results of this chapter have been published in [112]
[113]



Chapter

Five

CHAPTER 5

Conclusions and Future Work

5.1. Conclusions

The aim of this dissertation was to investigate the FPGA power consumption of the IFFT/FFT used in the OFDM model with the effects of different researched parameters. The investigation had analysed the result for the different parameters effect on FPGA power of IFFT/FFT part of the OFDM design.

The first stage of the investigation focused on the method used in OFDM power such as Fast-OFDM, ACP, and DSNR. These methods were focused on signal complexity, channel energy, and OFDM power with SNR. The DSNR find a relation with the FPGA power consumption of all OFDM model and the number of bits used in the calculation but not focusing IFFT/FFT. This thesis had focused on the FPGA power consumption of the IFFT/FFT used inside OFDM model to investigate the effect of using various parameters.

The second stage of this research discusses the FPGA evaluation board types, and the computer software program uses in the design of the OFDM model. Moreover, the power report generation procedure steps for the OFDM model design by Simulink Xilinx System Generator.

This report had included the FPGA power of each component of the design and focused on one part is IFFT/FFT.

There is two OFDM model implemented by the computer software Xilinx System Generator which are (complex and real) value OFDM. This software is developed by Xilinx and includes special tools to estimate the FPGA power consumption of the design. The OFDM model had implemented by Simulink Xilinx System Generator and collect the FPGA power of IFFT/FFT by the power report of the Simulink block. The result collected export to Excel software to draw the graph and compare the result.

The third stage of this thesis has investigated the researched parameters effects on the FPGA power consumption of the IFFT/FFT part in the OFDM design. In addition, the result has compared the power consumption of two model real and complex value OFDM. The real value IFFT used in real OFDM has been proposed in 1987 and was implemented in this dissertation. The researched parameters as follows:

- 1- **Bit precision:** The FPGA power consumption of IFFT inside OFDM transmitter has been increased with the increasing the number of bits used in the phase factor calculation. In the OFDM receiver side, the FFT power consumption by FPGA components was significantly increased with using more bit of precisions calculation. The two model implemented are (real and complex) value OFDM. The FPGA power consumption of the IFFT/FFT with precision from (16-32) bits the power is increased by 60% for complex IFFT/FFT.

However, the power consumption of the real value IFFT is increased by 41%, and for the FFT increased 57% with the same precision (16-32) bits.

The error rate between transmitted and received signal is decreased with increase in the IFFT/FFT precision calculation. Finally, the model built with low precision is better than high precision in term of FPGA power consumptions, but in term of error, the significant high precision is better.

- 2- **Cyclic prefix length:** It is used to reduce the intersymbol interference between OFDM symbols. The investigation is focused on Simulink block IP core IFFT from Xilinx which includes an option of CP. The CP increase will reduce the FPGA power consumption of the IFFT. This power reduction because of turn OFF the IFFT block power during the copy operations. Therefore, the average FPGA power used to generate OFDM symbols is reduced due to the power OFF period. The extended length of CP will reduce the FPGA power consumption of the OFDM and reduce the error rate between transmitter and receiver. However, the increasing length of CP is led to reducing bit rate because the CP does not carry any data. Finally, the long CP is better than the short in term of power consumption and error for both model built.
- 3- **FFT/IFFT length:** The FPGA power consumption has been increased with selecting the large size of the IFFT/FFT for both model real and

complex value OFDM. in addition, the large size of the IFFT/FFT required large FPGA chip area occupied.

However, the benefits of the large IFFT will processing more subcarriers input and increases the OFDM symbol length. The parallel input subcarriers data to IFFT depends on the IFFT size; the increased IFFT size is led to more parallel data to process inside the IFFT and increase the OFDM symbol. Finally, the increasing length of the IFFT will consumes more power but on the other side processing more subcarriers to produce long OFDM symbol and reduce the error.

- 4- **Subcarrier sampling frequency:** The investigation has been included in the sampling frequency of the subcarriers before input to the IFFT. The increasing sampling rate has increased the data rate of the subcarriers which is increased the speed of the processing. The processing of the IFFT/FFT increase is led to increase the FPGA power consumption. The FPGA power consumption of IFFT uses (QPSK and 16QAM) but different sampling rate. The power has increased when increasing the sampling rate for both real and complex value OFDM models. The benefits of increasing the sampling frequency which is increased the speed of the processing but increase the power consumption.
- 5- **Subcarrier modulation type:** The modulation type has been included as researched parameters affected on the OFDM power consumption. The changing of the modulation type to high order modulation from QPSK to 16QAM will increase the number of bits per subcarriers. The increasing number of bit per subcarrier need more processing to do the orthogonality between input subcarrier. More processing required

significant FPGA power inside IFFT/FFT. The comparison between subcarriers modulation QPSK and 16QAM with same bitrate 200Mb/s, the FPGA power of IFFT feed by 16QAM is lower than QPSK. However, when increasing bit rate to double for 16QAM, the IFFT power significantly increased and small difference in power 2% when using QPSK. Finally, higher modulation type is led to increase the FPGA power consumption but improve bit rate of the OFDM.

- 6- **Real and Complex OFDM model:** There is two OFDM model type built by depending on the IFFT output in the transmitter side. The output from IFFT was two parts the model called complex OFDM but when the output only real part the model called real OFDM. The experiment has been focused on the comparison FPGA power consumption between real and complex OFDM model. The FPGA power consumption by IFFT/FFT was lower in the real model than in complex with different parameters applied such as modulation type, IFFT size, sampling frequency, and cyclic prefix length.
- 7- **The word length width:** The mathematical bit precision represents the subcarriers of the OFDM before IFFT in computer software. The word length width has affected the FPGA power of the IFFT of the OFDM design. The power is increased with increasing number of bit used to represent word length of subcarriers because of increasing the processing inside IFFT with increasing width bits. The experiment implemented in this thesis with four length number of fixed type. The comparison is included different word length size fix16-15 which consumes 5.3mW compare with fix10-9 consumes 3.24mW. The

result shows the FPGA power of IFFT is decreased significantly with lower word length size.

The OFDM model build has included the researched parameters effect of IFFT power consumption. However, the OFDM design with higher order modulation such as 16QAM to 256QAM, sampling rate, and long length IFFT (1024) points long will increase the power consumption. The increasing power consumption of IFFT will increase the OFDM symbol length and increase data transmission per OFDM symbol when using 16QAM and QPSK. The result shows the same IFFT power consumption using 16QAM subcarriers input to IFFT and QPSK for same sampling frequency.

In addition, when increasing the length of IFFT will increase the length of OFDM symbol output, which increases the IFFT to double but does not double the power for both model complex and real value OFDM. The length of cyclic prefix effected on the power consumption of the IP core IFFT which reduce the power when increasing the length of CP. The increasing bit precision of the IFFT and word length width bit precisions of the subcarriers will increase the accuracy and increase the power consumption of IFFT/FFT. Finally, the real value IFFT consuming lower power (10-20)% than the complex value with a small difference in OFDM bit rate. The real FFT is consumed (30-50)% lower than complex value.

5.2. *Future Work*

It is proposed that the OFDM model design present in the previous chapters can be modified in the following

1. The stage of FPGA power consumption of IFFT/FFT has not considered the effect of the temperature. It will be interesting to investigate another parameter such effect of junction temperature, board layers, and board selection on the FPGA power consumption of IFFT/FFT for total and static power.
2. The OFDM model is focusing on IFFT/FFT power consumption, and it will be interesting to add a new parameter such as the switching activity, voltage supply source, timing analyses, and logic components, effect on FPGA power consumption of IFFT/FFT part.
3. This thesis included a researched parameters effect on FPGA power consumption of IFFT/FFT. It will be interesting to add the environment setting described in chapter three. The investigation includes the effect of environmental temperature, air flow, fan speed and heatsink on FPGA power consumption of IFFT/FFT. The spreadsheet from Xilinx is a good method to use and find the design worst case after modified the setting by the user and compare the result.
4. The effect of Adaptive Loading Algorithm (ALA) has not been implemented in this thesis. It will be interested to add (ALA) as a new parameter which is effect the FPGA power consumption on IFFT/FFT.
5. The Synchronisation part between the transmitter and receiver of the OFDM has not been implemented in this dissertation. This part needs

CHAPTER FIVE *CONCLUSIONS AND FUTURE WORK*

extra samples such as a preamble signal. It will be interesting to add the effect of the preamble signal on FPGA power consumption on IFFT/FFT of the OFDM model.

6. The RDFT is a low power model of the DFT it will be interested to apply the researched parameter on this part and study the effect of FPGA power consumption.
7. The Model built with Xilinx System Generator so it will be interesting to change the hardware evaluation board with optical terminal and use another program to implement such as Vivado.

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